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Three-stage control architecture for cascaded H-Bridge inverters in large-scale PV systems – Real time simulation validation

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HIGHLIGHTS

- Decentralized control architecture for a CHB Inverter in PV applications is proposed.
- Module level MPPT proposed in this work improves the transient response of system.
- Independent MPPT controls in phase level card provides better efficiency.
- CHB based PV-STATCOM operation is possible with the controls in master controller.

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ABSTRACT

In large-scale PV power stations, Cascaded H-Bridge (CHB) inverter based PV power conditioning systems are recommended over a conventional Two-Level Inverter based systems since CHB operates at medium voltage levels and provides better power quality. An insulated-gate bipolar transistor (IGBT) based H-bridge along with the auxiliaries such as DC link capacitors, breakers, contactors, bypass switch, voltage and current transducers is the fundamental power module of a CHB inverter. In this paper, the procedure for selection of components for Basic building block is presented. Due to a higher number of H-Bridge modules in a large-scale system, it is difficult to control the system with a single controller card. In this work, a control architecture for three-phase CHB based PV power conditioning systems is proposed in which the controls are distributed into three different stages. With the proposed control architecture, independent Maximum power point tracking (MPPT) controls of each PV array is carried out at module level itself. Carrying out MPPT controls at module level helps in improving the computational speed and in maintaining modularity. Hardware requirements of individual processor cards also minimized with the proposed control architecture. In this work, functionalities of each controller card namely module level control card, phase-level control card and master controller cards are explained in detail. Detailed interfacing and signal exchange between H-Bridge modules and the other controller cards are also presented. Controller-in-loop simulations are carried out with the help of Real-Time Simulator to validate the functionalities of each controller card. Real-Time simulation results are presented to verify the operation of the system with the proposed control architecture. Performance and dynamic response of MPPT controls for sudden changes in irradiance inputs on PV arrays are studied. Operation of the system during unequal irradiance inputs on the PV arrays is also analyzed. Current sharing between PV Inverter and grid to feed a fixed load for different values of irradiance inputs is explained through the presented results.

1. Introduction

With growing requirements in the renewable energy sector, solar PV power stations play a major role in providing green energy. In solar PV power stations, solar energy is converted into electrical energy through the PV array and the electrical energy is transferred to the grid or load

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through a power conditioning system (PCS). Since it is effective and flexible to utilize renewable energy through an inverter interfaced systems [1], a PCS consisting of an Inverter is used for transferring power from the DC side to the AC side. In large-scale PV systems, a conventional PCS based on a low voltage Two-Level inverter suffers from the following disadvantages (a) Since the system operates at low voltage, currents are high which increases the cost of the cable. (b) Due to high currents through power devices, conduction losses in the power devices are also more. (c) High amount of current through devices limits the switching frequency of devices hence the sine filter size is more to meet the power quality requirements as per grid codes. (d) Conventional PCS is connected to one common PV array which comprises a series-parallel combination of multiple PV modules. So it is not possible to carry out independent maximum power point tracking of PV arrays which causes in the reduction of overall efficiency of the system. Hence a conventional PCS is suitable for Low power ratings but for Large-scale PV systems, it is preferred to have a PV power conditioning system with medium voltage multilevel inverter configurations to counter the power quality issues such as voltage and current harmonics, voltage fluctuations, etc. in grid-tied PV applications discussed in Refs. [2,3]. Various multilevel voltage source inverter configurations such as neutral point clamped inverter, flying capacitor type multilevel inverters; cascaded H-Bridge multilevel inverters, etc. are discussed and compared in Refs. [4,5]. From the above studies, it is observed that the Cascaded H-Bridge based multilevel inverter topology is very popular for medium voltage, high power applications. Since independent DC sources are available in PV power station, cascaded H-Bridge (CHB) inverter based power conditioning systems are preferable over other multilevel inverter topologies.

Even though the control complexity and controller hardware requirements are more, CHB inverter is more preferred for large-scale PV systems due to following advantages (a) Since CHB inverter requires independent DC sources for each H-Bridge, PV arrays with smaller rating can be connected to each H-Bridge module which helps in carrying out independent MPPT control of PV arrays [6]. (b) Due to higher number of levels in the output voltage of a CHB inverter; good THD and power quality can be achieved [7]. (c) The system can be extended to higher power levels by incorporating additional H-Bridge units [8]. (d) Size of output filter can be reduced due to higher number of levels and higher switching frequencies. (e) Manufacturing and maintenance of CHB inverter are simpler compared to other multi-level inverters as the CHB inverter is modular in structure [9]. (f) For same power rating, cost of the power devices required for a conventional Two-Level inverter and the CHB inverter are almost equal. (g) Cost of the cable on the AC side is less compared to that of a two-level inverter. (h) With CHB configuration, it is possible to build a Transformer less power conditioning system which can further reduce the system cost.

With CHB based systems, Independent MPPT controls for each PV array is possible [6,10]. Since the current through each H-Bridge in a CHB inverter is same, the independent power through H-Bridges is regulated by controlling voltage output of each H-Bridge and the voltage output of each H-Bridge module is proportional to the irradiance input on the corresponding PV Array [11,12].

In present work, CHB inverter based solar PCS, the design of basic building block, selection of components are discussed. Since a CHB inverter consists of multiple PV arrays, the MPPT of each module with a common controller will affect the speed of computing or processing. Decentralized control architecture for CHB inverter which consists of two controller stages namely local controllers at the module level and a common master controller is presented in Ref. [13]. The proposed architecture is validated experimentally on a three-phase five level CHB inverter and concluded that the architecture proposed is useful in mitigating the practical non-idealities, reducing communication delays. System for PV applications and MPPT controls in the local controller are not covered in this work. Similar control architecture for STATCOM applications is discussed and validated on a single phase 7-level CHB based D-STATCOM in Ref. [14].

In Ref. [15], a distributed control architecture namely Inverter Molecule™ for PV applications is discussed and validated experimentally on a single phase 5-level CHB based PV inverter and concluded that the proposed control architecture gives better efficiency and reliability than the conventional control architecture.

The control architectures proposed in Refs. [13–15] are suitable for the systems with a lower number of H-bridges, but in case of large-scale systems when H-bridge modules are more in number, then additional control stages or different communication protocols may be required between the master controller and the local controllers. In Ref. [16], control architecture with CAN communication between cell controllers and the master controller is presented for large-scale systems. The proposed control architecture is implemented for a three-phase, 13-level CHB inverter for variable frequency drive applications.

In previous works mentioned above, distributed control architecture for CHB inverters, advantages such as improvement in computational speed, attaining modularity in controls, improvement in efficiency and reliability are discussed in detail. But these works are not focused on PV applications. The present work mainly focuses on the control architecture for large-scale PV applications. The proposed control architecture showed in Fig. 1 with three stages namely module-level

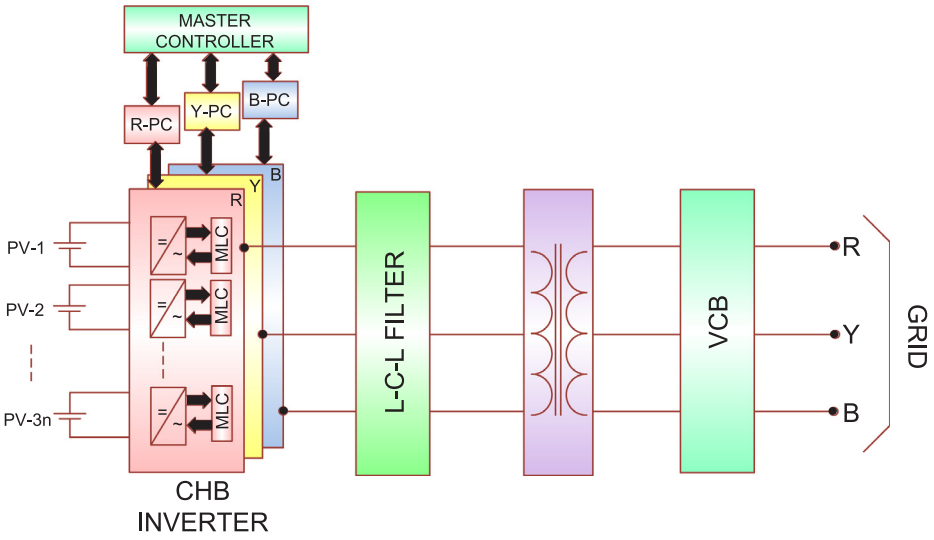

Fig. 1. Block diagram of a Grid-connected CHB based PV-Inverter.

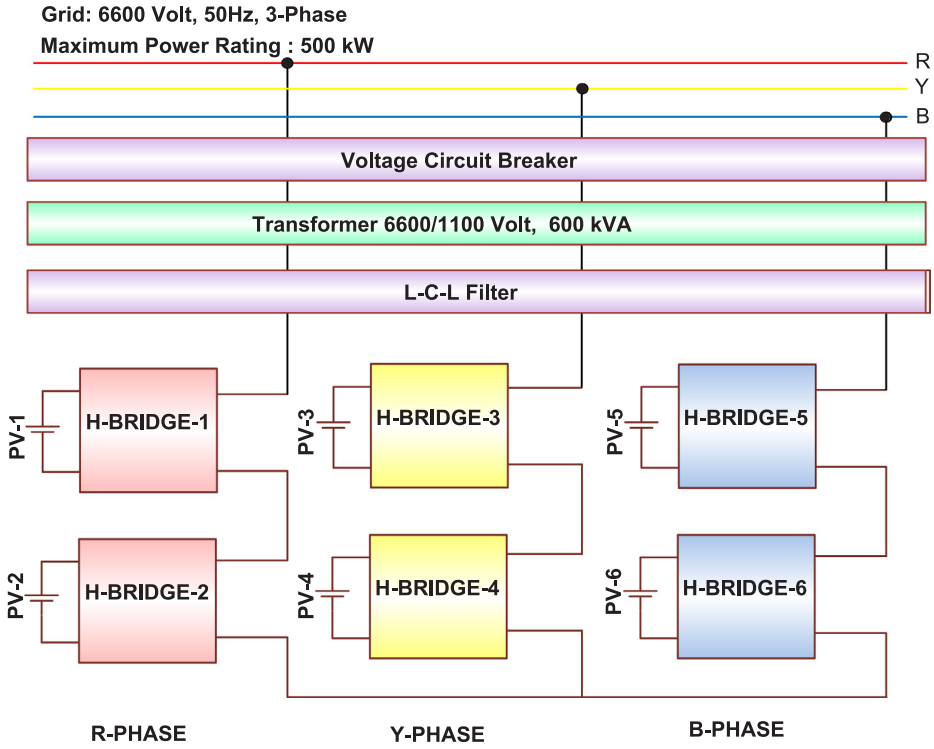

Fig. 2. CHB based PV-Inverter for Grid Connected System.

controller, phase-level controller and the master controller has the following advantages (a) Hardware requirement of controller cards is minimized and hence system cost is reduced. (b) Signals to be processed at each level of controls are minimized hence improves the processing speed. (c) MPPT controls of each PV array can be controlled independently at module level itself hence the efficiency can be improved. (d) Reference power generation through digital signals proposed in this work improves the speed of MPPT. (e) The proposed gate pulse generation at the module level enables the operation at higher switching frequencies, hence the power quality can be improved. (f) Modularity of the system increases hence the system can be extended to higher voltage and power levels by incorporating additional Modules without software changes. It is also possible to bypass a faulty module to operate the system at reduced power levels. (g) The controls implemented at the higher level of controls enable the feature of reactive power compensation.

In present system, Each H-Bridge module is interfaced with a module level controller card (MLC). The MLC performs functionalities such as MPPT controls of corresponding PV array, firing of IGBTs in H-Bridge module, control of PV switch and control of bypass switches in case if the module is faulty. Each H-Bridge module along with an MLC can be operated as an independent single-phase PV inverter of lesser power rating. Design of basic building block, the signal exchange between power circuit and module level controller card, controls at module level are discussed in Section 2.

In the proposed control architecture, all the MLC cards of one phase of a CHB inverter are interfaced with a phase level controller card (PC). Three number of Phase controller cards are required in a three-phase system. The main function of the PC is gate pulse generation for each H-Bridge module. Detailed discussions on the phase level controller card, signal exchange with module level controller cards, controls at phase level card are discussed in Section 3.

Three numbers of phase controller cards are interfaced with the Master controller. Master controller receives the signals such as grid voltages and currents for regulating the power flow through the PV inverter. Based on reference power, reference phase voltages are obtained in the master controller and the same is communicated to the corresponding phase level controller cards. Detailed discussions on the master controller card, signal exchange between master controllers with the phase level controller cards, controls at master controller card are discussed in Section 4.

Controller-in-loop simulation validation for the proposed system and controls are presented in Section 5. The system shown in Fig. 2 is selected as a case study to explain the design, operation, and controls of the proposed system and control architecture. The proposed control architecture and the controls are validated through the controller in loop simulations using a real-time simulator.

2. Basic building block with module level controller card

In this section, Design of basic building block of CHB inverter is discussed in detail. Since the Transformer secondary voltage is 1100 V, the phase voltage of the system is 635 V. Two numbers of H-Bridge modules are selected in the present system hence the AC voltage output of each H-Bridge module is 318 V and the minimum DC link voltage required is 432 V. Since the maximum power that can be transferred to the grid is 500 kW, each PV array with the rating of 100 kWp is selected as shown in Table 1. Determination of PV-to-inverter sizing is explained in [17].

2.1. Basic building block of CHB inverter

Fig. 3 shows the basic building block of a CHB inverter. This module comprises of an IGBT based H-Bridge, Thyristor based static bypass switch, DC voltage transducer, DC current transducer, DC contactor, pre-charge contactor and the bypass contactor. Module level card is also the integral part of H-Bridge module. When a start command is received from the higher level controller or from the user, then the PV switch is to be switched on. Before switching on the main DC contactor, a pre-charge contactor which is required to pre-charge the DC link capacitor is operated. Controller card provides the digital signals to operate these DC switches. The current rating of main DC contactor is selected around 250 A by considering the maximum power rating of each PV array at the minimum DC link voltage. IGBT current rating selected is 600 A which is almost double the rated current of each H-Bridge module.

Table 1
Electrical ratings of H-Bridge module.

Electrical parameter	Value	Units	Description
Inverter AC Side Voltage (Vac)	1100	V	Three Phase
Maximum PV Power	500	kWp	
Phase Voltage (Vphase)	635	V	Vac/1.732
No of H-Bridges per phase (N)	2	No's	2H-Bridges per phase are selected
No of PV arrays	6	No's	N × 3 Phase
AC voltage of each H-Bridge (Vac_H)	318	V	Vphase/N
Minimum DC Link Voltage	432	V	1.35 × Vac_H
Peak power of each PV array (Ppv)	100	kW	> 500 kWp/N
RMS Current of H-Bridge	315	A	Ppv/Vac_H
No. of levels in Phase voltage	5	Levels	2 N + 1
No. of levels in Line Voltage	9	Levels	4 N + 1

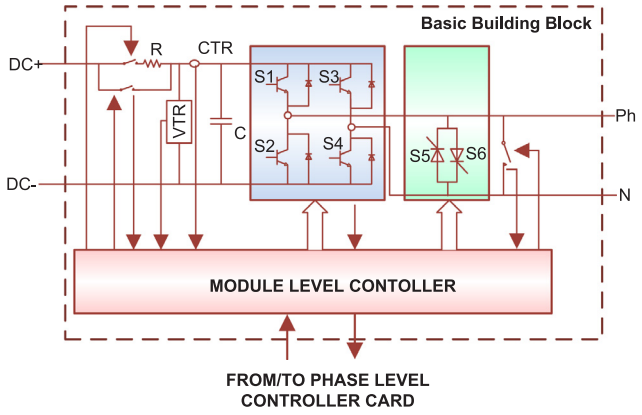

Fig. 3. Block diagram of building block for CHB inverter.

Design of IGBT based inverters is explained Ref. [18] and power loss calculations for a grid-connected CHB inverter are discussed in [19,20].

Gate signals from the controller card are given to the gate driver card of IGBT and a common H-Bridge fault is given to the controller card. A thyristor-based bypass switch is used in the H-Bridge module which is required to bypass the IGBTs instantaneously when there is a fault in H-Bridge. Bypass contactor will be switched on subsequently. If thyristors are to be operated for continuous operation then the device losses and switching losses will be more, hence a bypass contactor is used in parallel to the thyristor switch. Thyristors are selected for short time operation with a rated current almost equal to the IGBT rated current. Controller card also provides digital signals to operate bypass switch components. PV array voltage and currents are monitored by the controller card through DC voltage and DC current transducers respectively. These signals are required for the controller to track the maximum power point of associated PV array.

2.2. Functionalities of module level controller card

2.2.1. Operation of pre-charge and main DC contactors

Module-Level controller card monitors signals such as start command from the user, DC link voltage and the main DC contactor ON/OFF status indication as shown in Fig. 4. When the start command is received from the Phase level card, then the PV array needs to be connected to the DC link of H-Bridge. To switch on the main DC contactor, the following actions are taken by the controller.

- In case if the DC link voltage is Zero or less than the minimum DC link voltage then the pre-charge DC contractor is switched ON. Then DC link capacitors are charged slowly from PV source through pre-charging resistors connected in series with the pre-charging contactor.
- Once the DC link voltage reaches to its minimum DC link voltage required, then the ON command is given to the main DC contactor.
- On receiving the DC contactor ON status signal to the controller, the controller switches OFF the pre-charge contactor.

2.2.2. Maximum power point tracking

The main functionality of the module level controller card is tracking the maximum power point (MPP) of the associated PV array connected to DC link. the following actions are taken by the controller for MPPT

- MLC monitors the PV voltage and PV current
- Perturb and observe (P&O) method of MPPT shown in Fig. 5 is adapted in the present system. Based on new reference power and the present PV power, increase or decrease power reference (Pinc and Pdec) commands will be sent to the higher level controller card.
- Pinc and Pdec signals are digital signals. Higher level controller card obtains the reference power by integrating the Pinc – Pdec signal.

2.2.3. Gate pulse distribution

Since the CHB inverter in grid-connected applications always operates at a fixed frequency, it is possible to derive four gate signals from one gate signal received from the higher level controller as shown in Fig. 6. A fixed frequency of 50 Hz is assumed in this system

- On receiving Gate signal from higher level controller card, the same signal is given to the IGBT switch S1. Gate Signal of S1 is inverted and given to the IGBT switch S2.
- Gate Signals of S1 is delayed by 180 degree electrical and applied to

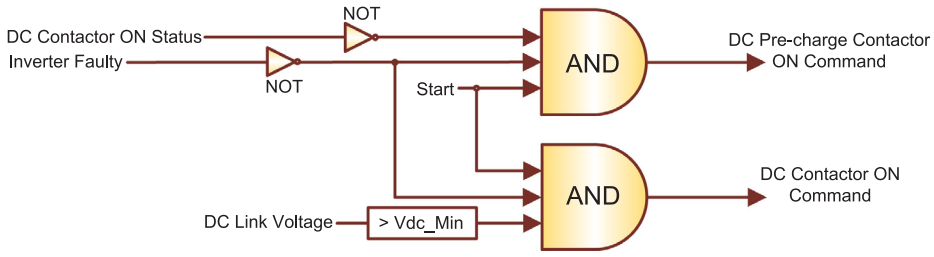

Fig. 4. The operational logic for Pre-charge and main DC Contactors.

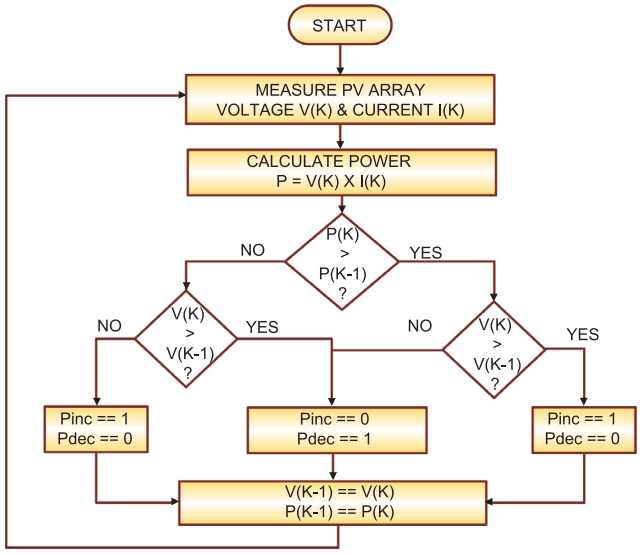

Fig. 5. The operational logic for Perturbation & Observation Method of Maximum power point tracking.

the IGBT switch S3. Gate Signal of S3 is inverted and given to the IGBT switch S4.

- Each Gate pulse is chopped at the leading edge to create a dead band between top and bottom switches in one leg of the H-Bridge. Dead band of 6 μs is applied in this work.

2.2.4. Operation of bypass module

Module level controller card operates the bypass switch components such as thyristors and bypass contactor during H-Bridge fault to ensure the continuous operation of the system as shown in Fig. 7. The following activities are carried out by the controller card to bypass an H-bridge module

- If the inverter fault signal becomes high, then the controller Block gate pulse to the H-Bridge
- Gate pulse for the thyristor-based static bypass switch and bypass contactor are released by the controller.
- 500 Hz rectangular pulses with 50% duty cycle are given as gate pulse to the thyristors through driver cards consisting of isolated pulse transformers.
- Due to faster switching, thyristors switch ON immediately and bypasses the H-bridge.

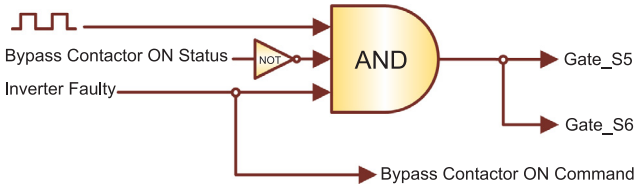

Fig. 7. The operational logic for bypass switch components.

- Bypass contactor switches ON subsequently based on the time constant of coil operated contactor.
- Once the bypass contactor ON status signal is received, the thyristor gate pulses are blocked by the controller.

In this work, Perturb and Observe method of MPPT is considered for ease of understanding. Various MPPT Techniques such as constant voltage method, open circuit voltage method, Short circuit current method, perturb and observe (P&O) method, incremental conductance (IC) method, etc. are existing and among these, IC method and P&O methods are popularly used MPPT techniques due to high accuracy and good dynamic performance during sudden changes in climatic conditions [21,22]. Performance of the above two techniques are compared with each other for dynamic weather conditions in Ref. [23] and it is observed that IC method is slightly superior to P&O method but both methods are not efficient at low Irradiance inputs. In this system, adaptive MPPT techniques explained in Refs. [24,25], dual MPPT algorithm explained in Ref. [26], Tangent error method of MPPT explained in Ref. [27], Taguchi method of MPPT algorithm explained in Ref. [28], etc. can also be implemented with minor modifications.

2.3. Signal exchange and hardware requirement of module level control card

Module level controller card receives and transmits signals from/to the H-Bridge module and the Phase-Level controller card. In this work, the controller card selected as module level controller is based on a TMS320F2812 DSP processor and the block diagram of the selected controller card is as shown in Fig. 8. Suitable signal conditioning circuitry and the voltage attenuation circuits are used to match the voltage levels of DSP card with the other components such as voltage transducers, current transducers, gate drivers and other controller cards. Summary of signals at Module level controller card and the significance of each signal are described below. Digital and analog Input /Output channels requirement at module level controller card is summarized in Table 2.

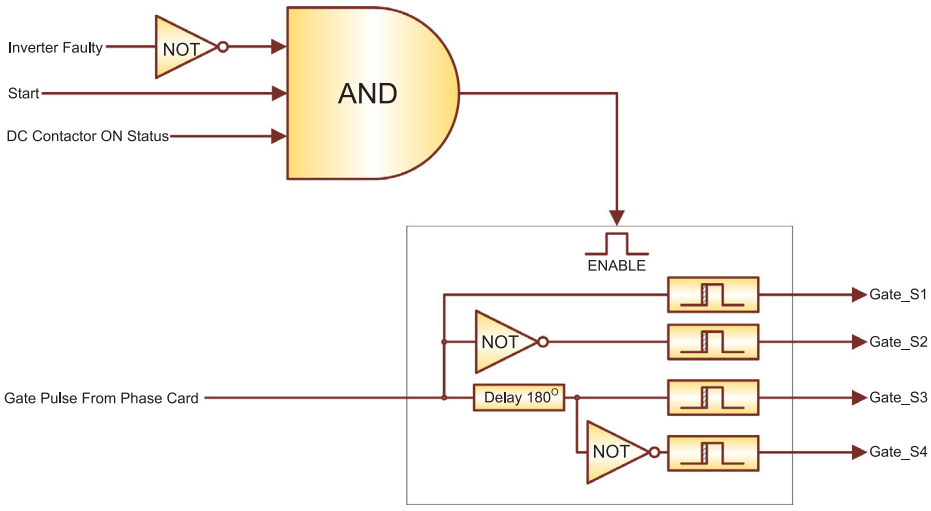

Fig. 6. The operational logic for IGBT Gate pulse distribution in Module-Level Control card.

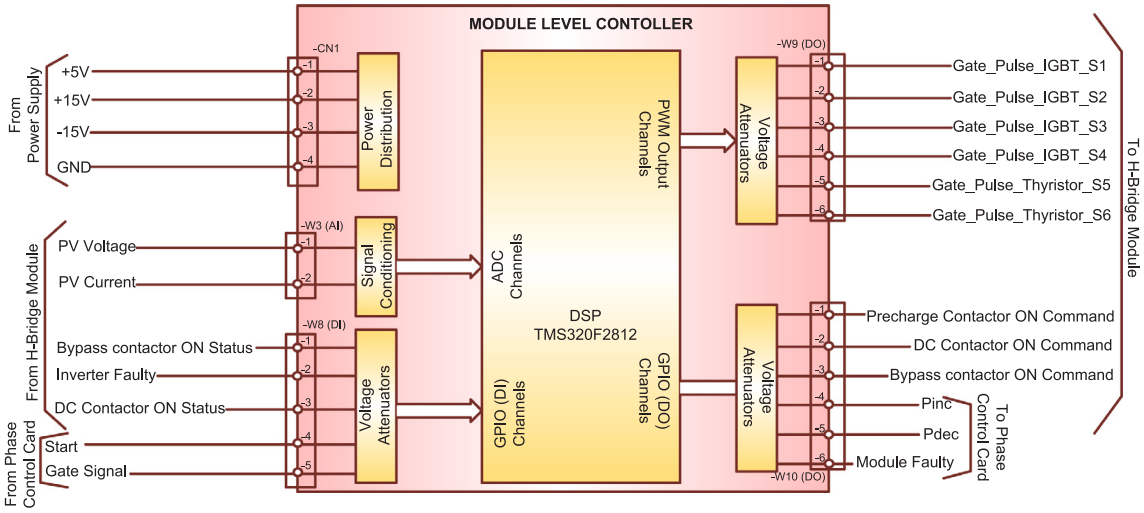

Fig. 8. Signal Exchange diagram of Module level control card.

Table 2
List of input/output channels required at module level control card.

Type	Number of I/O channels	Voltage level
Digital Inputs (DI)	5	0 V = Logic Low, 15 V = Logic High
Digital Outputs (DO)	12	0 V = Logic Low, 15 V = Logic High
Analogue Inputs (AI)	2	−10 V to +10 V
Analogue Outputs (AO)	0	−10 V to +10 V

- **Start Command:** This digital signal received from the phase controller card initiates the process flow in the module level controller.
- **Pre-charge Contactor ON Command:** This digital output signal from the module level controller card switches on the Pre-charge contactor in the H-Bridge module.
- **DC Contactor ON Command:** This digital output signal from the module level controller card switches on the main DC contactor in the H-Bridge module.
- **DC Contactor ON Status:** On receiving this digital input signal from the H-Bridge module, Power control to the Grid is enabled.
- **PV Voltage and PV Current:** These Analog input signals from the H-bridge module are required for tracking of Maximum power point.
- **Increase reference Power (Pinc):** This is a digital output signal to be given to the phase controller card. This signal is high when the new power reference is more than previous power reference.
- **Decrease reference Power (Pdec):** This is a digital output signal to be given to the phase controller card. This signal is high when the new power reference is less than previous power reference.
- **Gate Signal Input:** Based on new power reference, Gate pulse for each H-Bridge module is obtained in Phase Controller card and given to the module level controller card as a digital input.
- **Inverter Gate Signals:** 4 No's of gate signals are derived from the Gate signal input received from the phase controller card. The generated inverter gate signals are given to the H-Bridge module through digital output channels of the module-level controller card.
- **Inverter Faulty:** This digital input signal is received from IGBT H-Bridge in case of occurrences of faults such as high temperature, short circuit fault etc…
- **Module Faulty:** This digital out signal is given to the phase controller card. This signal is enabled on receiving the inverter faulty signal becomes high.
- **Static Bypass Switch Gate:** Two digital output channels in module level controller card are used for providing Gate Signals to gate driver card of thyristor switches on receipt of inverter faulty signal from H-bridge module.
- **Bypass Contactor ON Command:** This digital output signal from the module level controller card switches on the Bypass contactor in

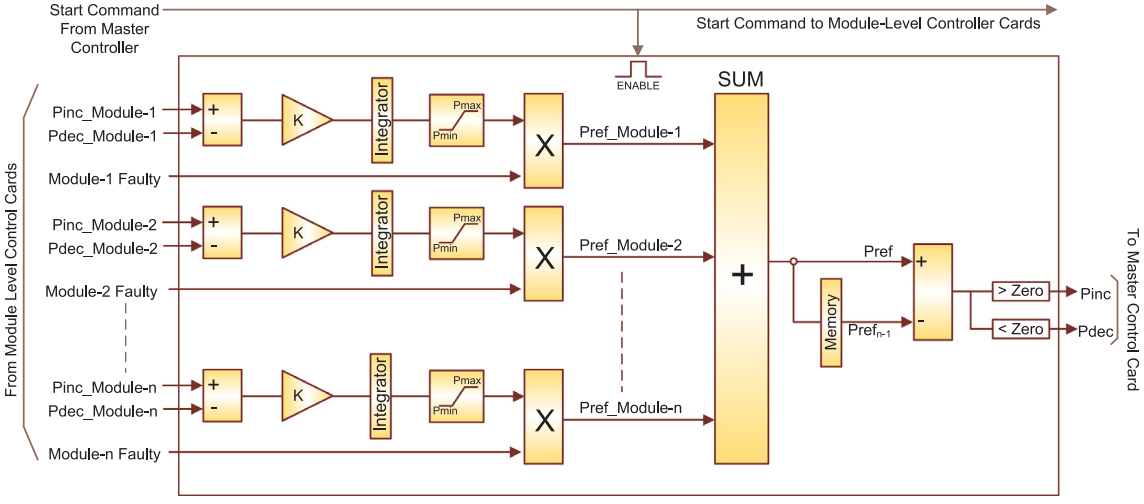

Fig. 9. The logic for reference power generation in phase level control card.

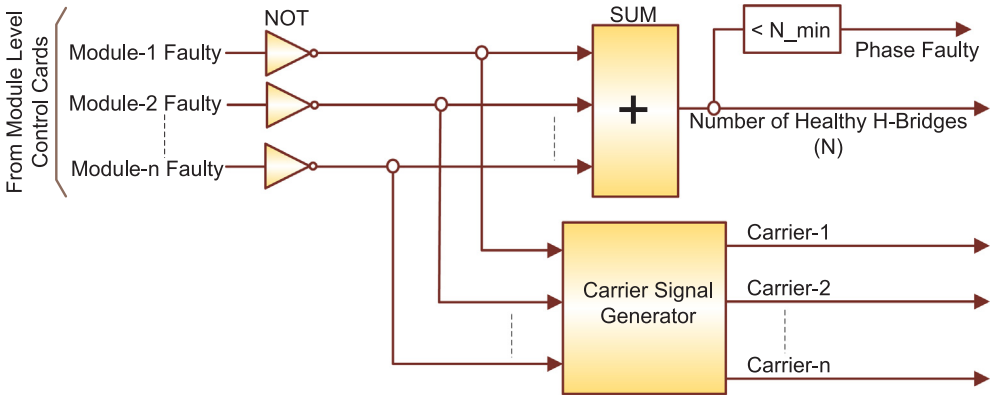

Fig. 10. The logic for generating Carrier signals and phase faulty signal in phase level control card.

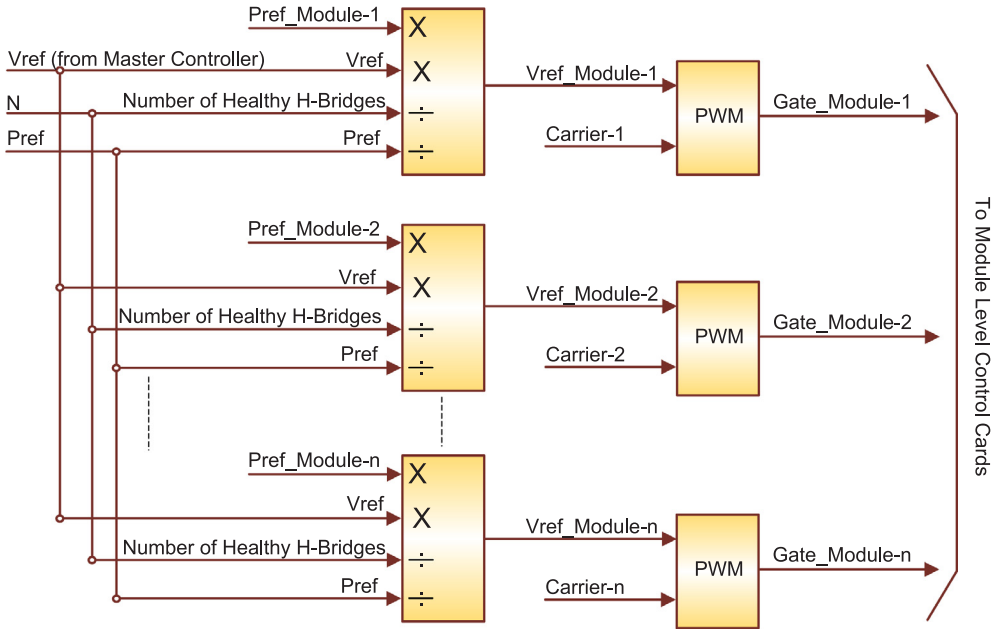

Fig. 11. The logic for Gate Pulse generation for each Module-level card.

Table 3
List of input/output channels required at phase control card.

I/O Channel Type	Number of I/O Channels						
	Qty	N = 1	N = 2	N = 3	N = 4	N = 5	N = 6
Digital Inputs (DI)	1 + 3(N)	4	7	10	13	16	19
Digital Outputs (DO)	3 + 2(N)	5	7	9	11	13	15
Analogue Inputs (AI)	1	1	1	1	1	1	1
Analogue Outputs (AO)	0	0	0	0	0	0	0

the H-Bridge module on receipt of inverter faulty signal from H-bridge module.

- **Bypass Contactor ON Status:** On receipt of his digital input signal from H-bridge module, gate signals for thyristor based static bypass switch are blocked

3. Phase level control card

Three numbers of phase controllers are to be used for a three-phase system and each phase control card is interfaced with the corresponding module level controller cards. All three-phase controller cards are interfaced with the master controller card.

3.1. Functionalities of phase level controller card

Phase level controller receives the start command and the reference voltage signal from the master controller and performs the following functions

3.1.1. Reference power generation

- By compiling Increase and decrease reference power signals received from all the corresponding MLC cards, overall reference power is obtained in the phase control card.
- From the obtained reference power, the phase controller card generates an overall increase/decrease reference power signal and

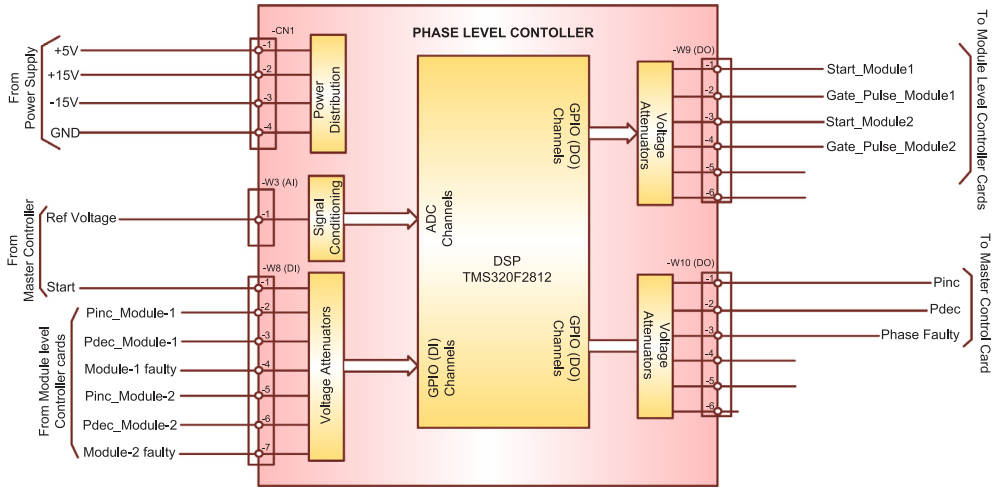

Fig. 12. Signal Exchange diagram of Phase level control card.

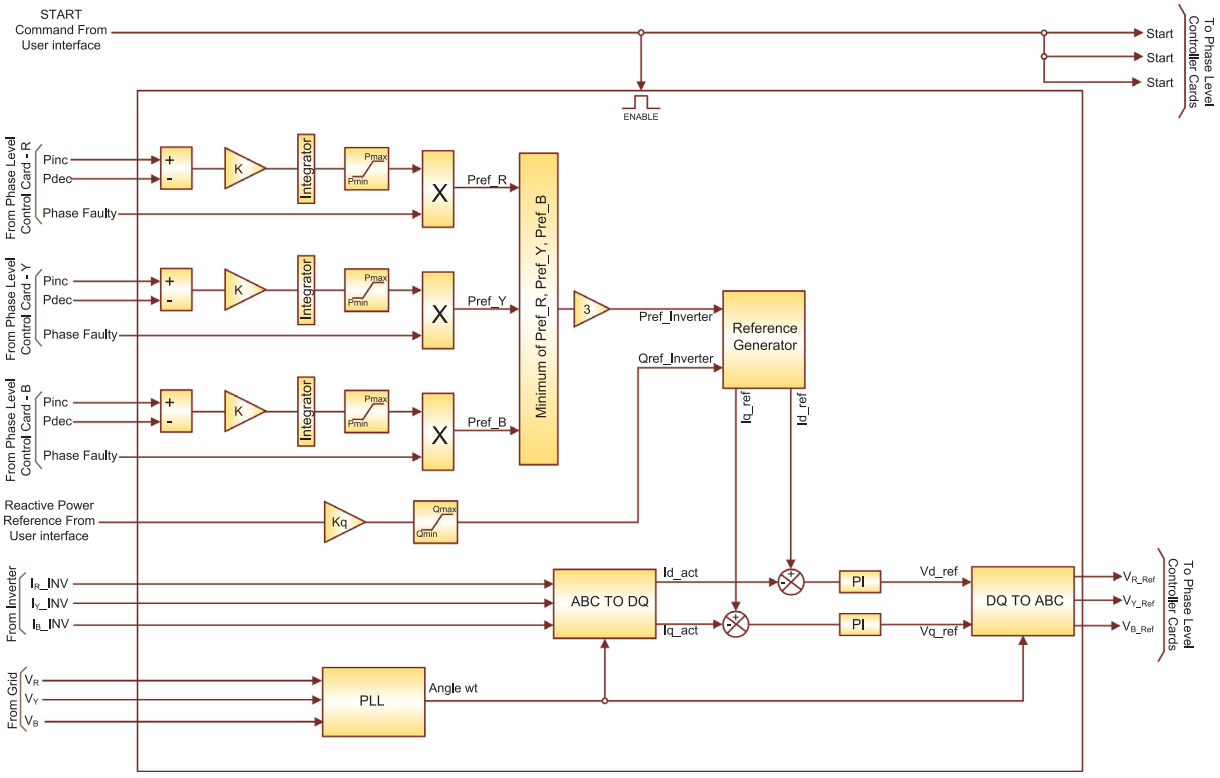

Fig. 13. A functional diagram of Master Controller Card.

provides the signal to the master controller card as shown in Fig. 9.

- In selected system, Since each PV array is rated for 100kWp; Pmax = 100 kW and Pmin = Zero.

3.1.2. Generation of phase faulty signal and carrier wave generation

- A phase faulty signal is generated in the phase controller card as shown in Fig. 10, when the number of Healthy H-Bridge modules is less than the minimum number of healthy modules (N_min) required for continuous operation.
- In case if the number of H-Bridges per phase is '6' and '2' H-bridge modules are faulty, still, the system can be made operational for the selected values of grid and PV voltages. If more than 2 number of H-bridge modules are faulty, then the phase faulty signal will be generated which necessities the troubleshooting of the inverter system.
- Carrier signals for each H-Bridge module are generated based on a number of healthy H-bridge modules

3.1.3. Gate pulse generation

- Reference modulating signals for each module is obtained from the

Table 4
List of input/output channels required at master control card.

Type	Number of I/O Channels
Digital Inputs (DI)	8
Digital Outputs (DO)	3
Analog Inputs (AI)	6
Analog Outputs (AO)	3

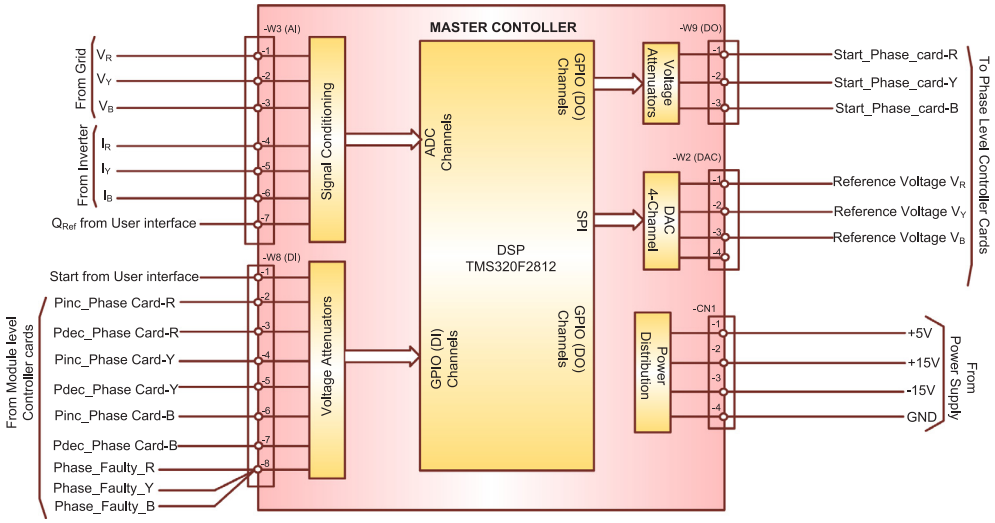

Fig. 14. Signal Exchange diagram of Master controller card.

reference powers of each module as shown in Fig. 11.

- One gate signal for each module is derived based on the modulating signal and the carrier signal.
- The phase shifted PWM technique is adopted in this work for pulse generation.

3.2. Signal exchange and controller hardware requirement

'N' number of MLC cards are interfaced with one Phase level card where 'N' is the number H-bridges per phase. In the present work, 2 No's of H-bridge modules per phase is selected. List of signals between Phase level controller card and each module level controller card and the significance of each signal is explained in an earlier section. List of signals between Phase level controller card and the master controller card and the description of each signal is explained as below

- **Start Command from Master Controller card:** This digital input signal is received from the master controller to initiate the processing in phase level controller card.
- **Reference Voltage to Phase controller card:** Through Current controller in the master controller, three-phase reference voltages are obtained. The master controller gives the corresponding voltage reference signal to the analog input channel of each phase controller card.
- **Increase reference power (Pinc) and Decrease reference power (Pdec):** Based on the Pinc and Pdec signals received from each Module level cards, a common Pinc and Pdec signal are generated and the same are transmitted to the master controller through digital output channels of phase level controller card. Master controller determines the reference power based on these signals.
- **Phase Faulty:** When the faulty H-Bridge modules are more in number, it is not possible to keep the system in operation. Then a phase faulty signal is generated and given to the master controller

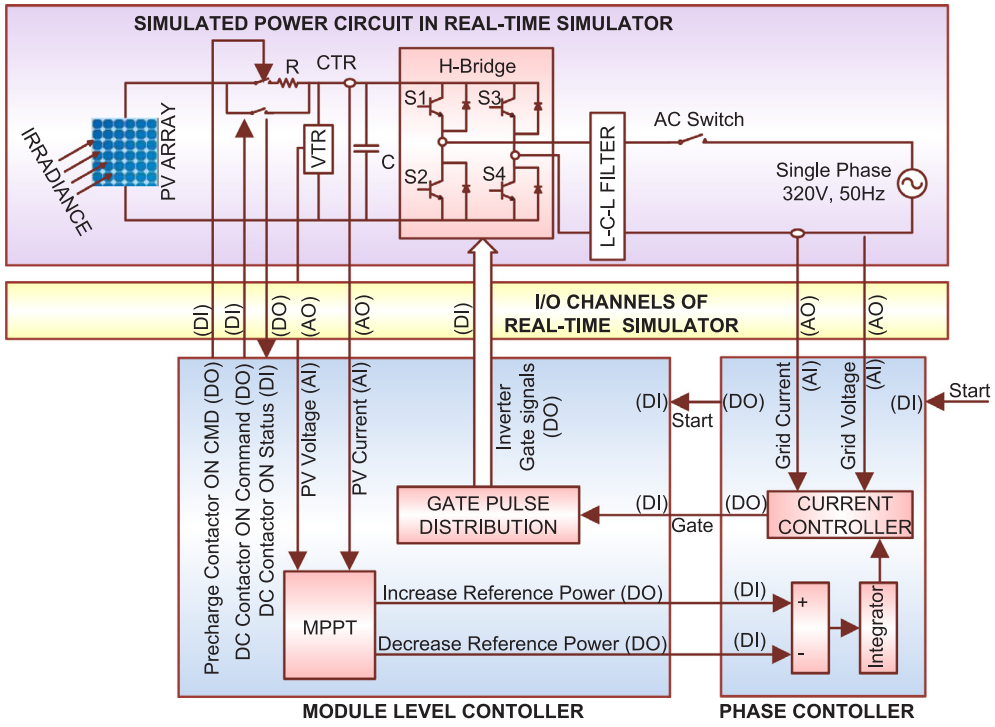

Fig. 15. Block diagram of Controller-In-Loop simulation validation of module-level controller card.

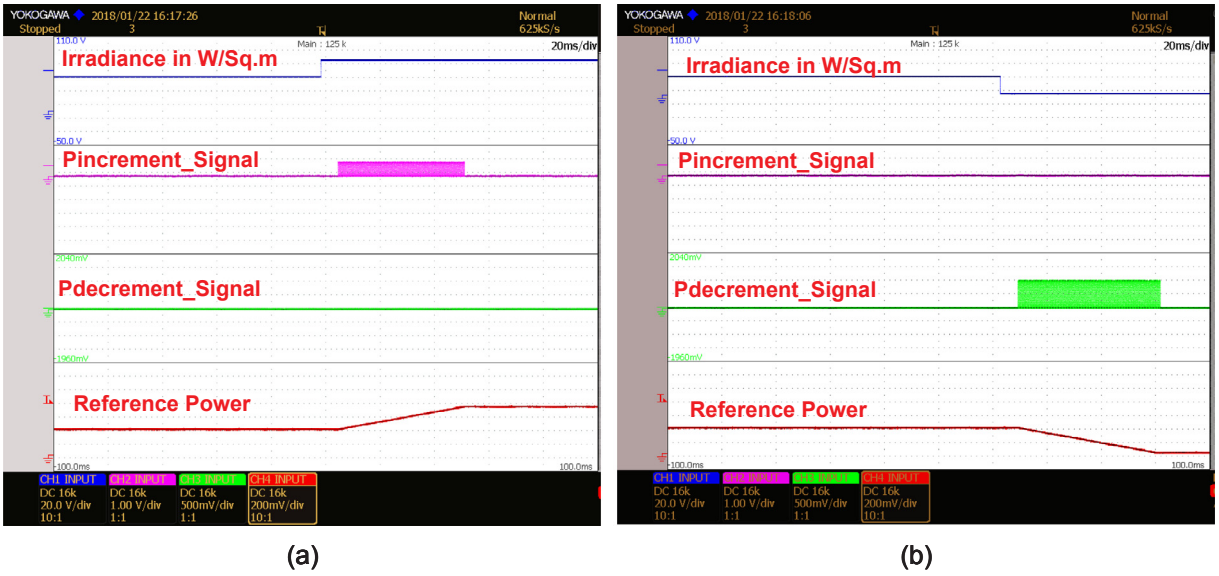

Fig. 16. (a) Increment/Decrement power reference Signals and the reference power during increment in the Irradiance input of PV array. (b) Increment/Decrement power reference Signals and the reference power during decrement in the Irradiance input of PV array.

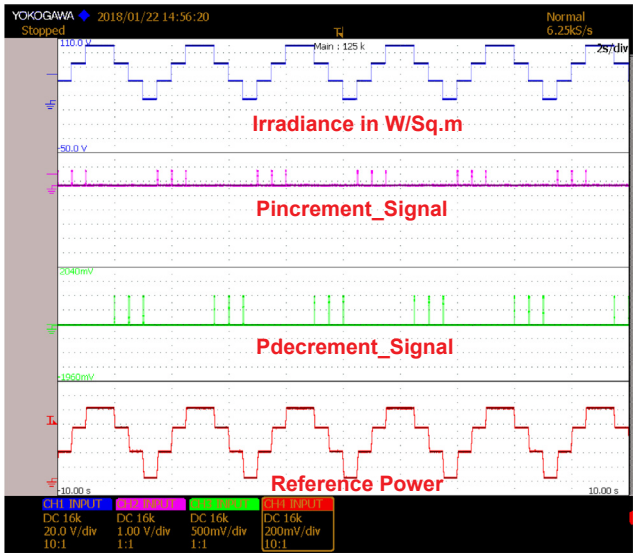

Fig. 17. Increment/Decrement power reference Signals and the reference power during step-change in the Irradiance input of PV array.

through a digital output channel of the phase controller card. Master controller safely shuts down the system on receiving this signal from any one phase-controller card.

Based on the above discussions, Digital and analog Input/output channels requirement at Phase level controller card is summarized in Table 3 for a different number of H-Bridge modules per phase. As mentioned earlier, the number of H-bridges per phase selected is Two and the controller hardware selected for the module level controller is only used for Phase-level controller card also. Block diagram of the phase controller card and the I/O channel allocation for the signal exchange are shown in Fig. 12.

4. Master controller

In the previous section, functionalities of phase controller card and hardware requirements for the phase controller card are explained in detail. Three such phase controllers are interfaced with the master controller in a three-phase system. Functionalities, Hardware requirement and signal exchange at master controller are presented in this section. Controls presented in Ref. [29] are implemented in the master controller for the power transfer through the CHB based PV inverter.

4.1. Functionalities

The following are the functionalities carried out in the master controller

- Calculation of Reference Inverter Power: As discussed in earlier sections, a master controller card receives an increase and decrease power reference signals from three phase controller cards. The master controller processes these signals and obtains the reference power of each phase as shown in Fig. 13.
- To avoid unbalanced currents in the system, Inverter Power reference is obtained based on the Eq. (1) shown below

$$\text{Inverter Power reference} = 3 \times \text{Minimum of power reference obtained from three phases} \quad (1)$$

- In this work, since Two H-Bridge modules per phase are considered; Pmax = 2 × 100 kW and Pmin = Zero in Fig. 13.
- Reactive power compensation is also possible in this system and the reactive power reference can be adjusted by the user through an analog input channel. The concept of PV inverter used for reactive power compensation is known as PV-STATCOM [30]. Reactive power compensation through renewable energy systems is cost competitive when compared with switched capacitors [31].
- Calculation of Reference Inverter Current: Based on Reference active and reactive powers obtained above, direct and quadrature axis components of reference current is calculated. The phase angle required for Three-phase ABC to D-Q conversion is obtained through a phase-locked loop (PLL) shown in Fig. 13.
- Inverter Current Control: Reference d-q currents are compared with the d-q components of actual inverter currents and the error signals are given to the proportional-integral (PI) controllers to obtain the reference voltages Vd_ref and Vq_ref as shown in Fig. 13.
- The d-q components of reference voltages are converted into three-phase reference voltages. The obtained reference three-phase voltage signals are given to the corresponding phase controller cards.

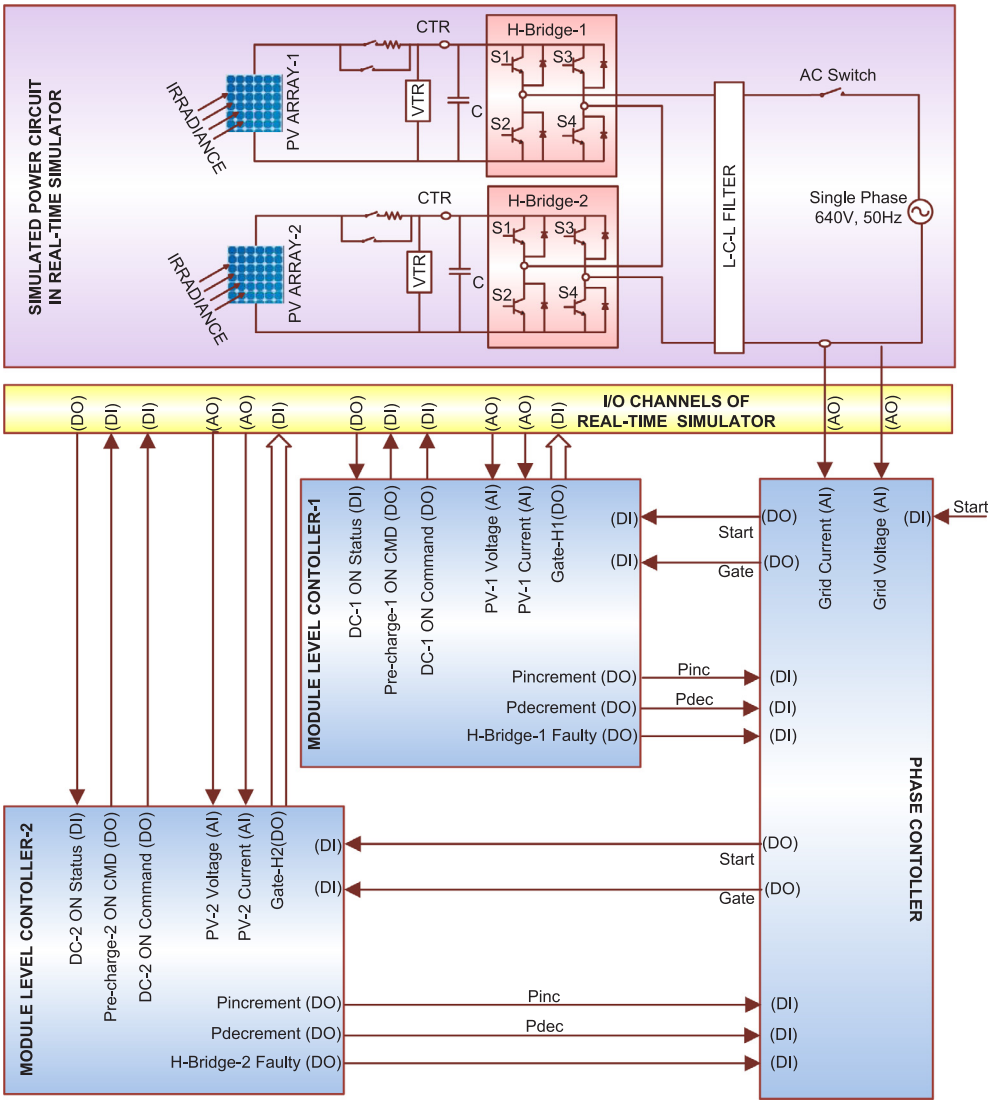

Fig. 18. Block diagram of Controller-In-Loop simulation validation of one Phase level controller card.

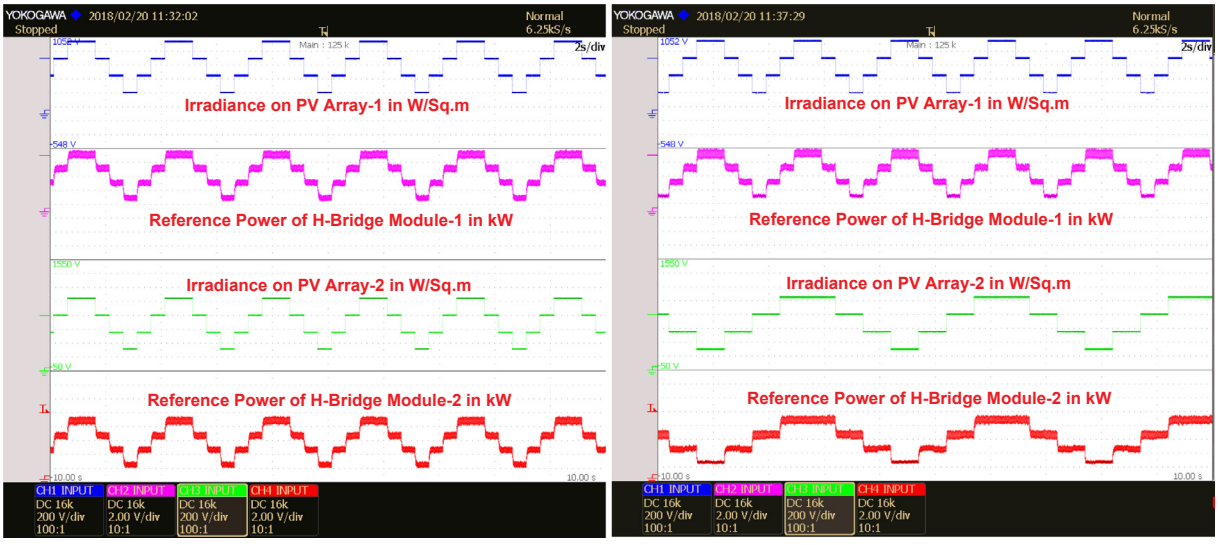

Fig. 19. (a) Reference Powers of H-Bridge modules for equal values of Irradiance on PV array-1 and PV Array-2 (b). Reference Powers of H-Bridge modules for unequal values of Irradiance on PV array-1 and PV Array-2.

Fig. 20. (a) Output PWM voltage of each H-Bridge module when the irradiance on PV-Array-1 is equal to that of PV-Array 2. (b) Output PWM voltage of each H-Bridge module when the irradiance on PV-Array-1 is more than that of PV-Array 2. (c) Output PWM voltage of each H-Bridge module when the irradiance on PV-Array-1 is less than that of PV-Array 2. (d) PWM Voltages of each H-bridge module and the CHB Inverter PWM Voltage.

4.2. Signal exchange and controller hardware requirement

Based on the above discussions in the previous subsection, digital and analog Input/output channel requirement at a master controller card is summarized in Table 4. The controller hardware selected for the module level and Phase-Level controllers is only used for Master controller card also. Three phase faulty signals are received at module level controller card one from each phase controller card. Since the reference inverter power becomes zero even when there is a fault in any one of the phase faulty signal becomes high. Hence three numbers of phase faulty signals are shorted and connected to one digital input channel instead of using three numbers of independent digital input channels. Serial peripheral interface (SPI) is programmed to transfer the reference voltage signals to the phase controller cards through external digital to analog converter circuit. Block diagram of the master controller card and the I/O channel allocation for the signal exchange are shown in Fig. 14.

5. Results and discussions

With the help of real-time simulations, it is easy to develop the preliminary controller software with minor assumptions in plant parameters and it helps in reduction of design time, design cost [32,33]. In this work, the proposed control architecture and the controls at different stages are validated through real-time simulations. An Opal-RT make real-time simulator is used in this study. Real controller hardware can be interfaced with the simulated power circuit with the help of Input/output channels of the Real-Time simulator. Since the real-time simulator is consisting of high-speed Intel Xeon Quad Core 2.50 GHz processor, the system operates as a real-time system.

5.1. Real-time simulation validation of module level controller card

To validate the functionalities of module-level controller card alone, controller-in-loop simulations for module level controller card interfaced with a single phase grid-connected PV power conditioning system is carried out as shown in Fig. 15. The power circuit comprises of the basic H-Bridge module fed from a PV array explained in earlier subsection connected to a single phase 320 V Grid through an L-C-L filter and an AC contactor. A bypass switch is not used in the basic building block since only one H-bridge module is used. The basic functionalities required at module levels such as Gate-pulse distribution, MPPT controls and switching of DC contactors are programmed in the module level controller card. One phase controller is used for the power control through an inverter.

As explained in earlier subsections, the Module level controller card performs the MPPT controls and the increment/decrement power

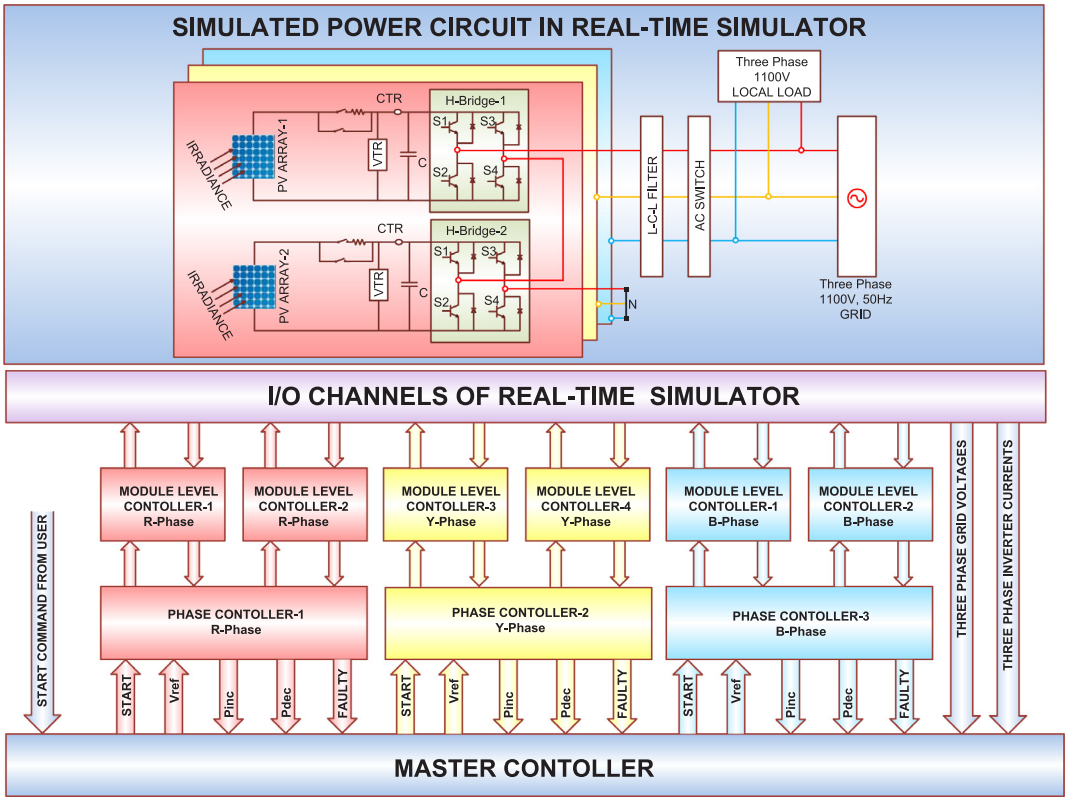

Fig. 21. Block diagram of Controller-In-Loop simulation validation of Master controller card.

reference signals are given to the phase controller. Fig. 16 shows the 'Pinc' and 'Pdec' signal generation in the module level controller card for a step change in irradiance input on the PV array and the generation of reference power signal in the phase controller card. The following activities are carried out during validation through controller-in-loop simulations.

- The power circuit is simulated, compiled and loaded in the CPU of the Real-Time simulator.
- Module level controller and Phase controller cards are loaded with the application programme.
- A step change in irradiance value is applied and to monitor the irradiance value in an oscilloscope, Irradiance value is given to an Analog output channel of the real-time simulator.
- Module level controller monitors the PV voltage and current for MPPT and generates 'Pinc' and 'Pdec' signals. The generated digital output signals are given to the phase controller and also monitored in the oscilloscope.
- On receiving 'Pinc' and 'Pdec' signals, the phase controller card generates the reference power value through an integrator. The reference power value is given to a digital to analog converter (DAC) through a serial peripheral interface (SPI) of DSP. The output of DAC is given to the oscilloscope to monitor the reference power signal.

Maximum PV array Power Rating = 100 kW
Step change in Power during MPPT = 100 W

$$\text{Reference power} = P(n-1) + (Pinc - Pdec) \times 100\ \text{W} \quad (2)$$

where

Pn is Inverter power reference,

P(n − 1) is Inverter power reference at previous sample time,

Pinc is "Increase the reference power" signal generated in the Module level controller card,

Pdec is "Decrease the reference power" signal generated in the Module level controller card.

In Eq. (2), initially 'P(n − 1)' is Zero and when the Irradiance is increased, 'Pinc' signal is generated and accordingly the reference power is increased gradually as shown in Figs. 16(a) and 17. Similarly, when the irradiance is reduced, 'Pdec' signal is generated and accordingly the reference module power is reduced gradually as shown in Figs. 16(b) and 17. Irradiance value in the power circuit is varied from Zero to 1000 W/sq m in steps of 250 W/sq m as shown in Fig. 17. To monitor in an oscilloscope, Irradiance value is given to an Analog output channel of the real-time simulator.

From the real-time simulation results presented, it is observed that the dynamic response of the MPPT controls for sudden changes in the irradiance is satisfactory as the system obtains the new reference power in very short time i.e. approximately in 40–50 ms for an irradiance change of 250 W/sq m. In comparison with the simulated adaptive MPPT methods presented in Refs. [34,35], the present MPPT technique programmed in module level and phase level controller card results in obtaining slightly enhanced performance. Hence it is assured that the module level controller and the associated control software are functioning properly.

In this system, increase and decrease reference power signals is given to the digital input channels of the phase controller card to determine the power reference. However, if an external digital to analog converter is available in the module level controller card, then the power reference can be determined in the module level controller card itself and the value can be given to the phase controller card through an analog output channel of the module-level controller card. From this study, it is evident that each H-Bridge module can be used independently also for low power, single phase residential applications. As a future work, it is possible to incorporate a battery energy storage system and its controls at module level with minor modifications in the presented control philosophy.

5.2. Real-time simulation validation of phase level controller card

To validate the functionalities of a phase level controller card,

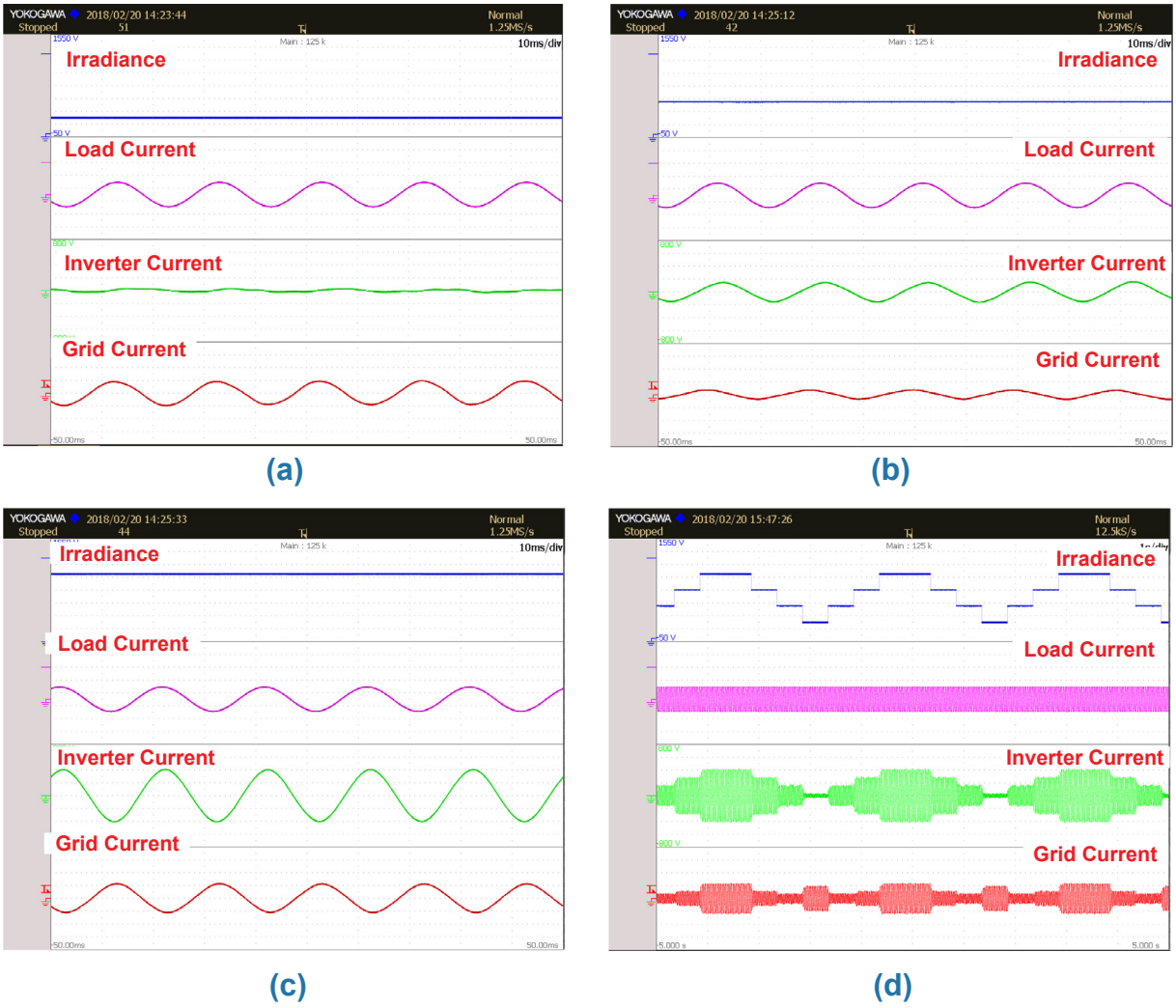

Fig. 22. (a) Load Current, Inverter current and Grid current when irradiance is Zero W/sq m. (b) Load Current, Inverter current and Grid current when irradiance is 250 W/sq m. (c) Load Current, Inverter current and Grid current when irradiance is 750 W/sq m. (d) Steady-state Load Current, Inverter current, and Grid current for different values of irradiance.

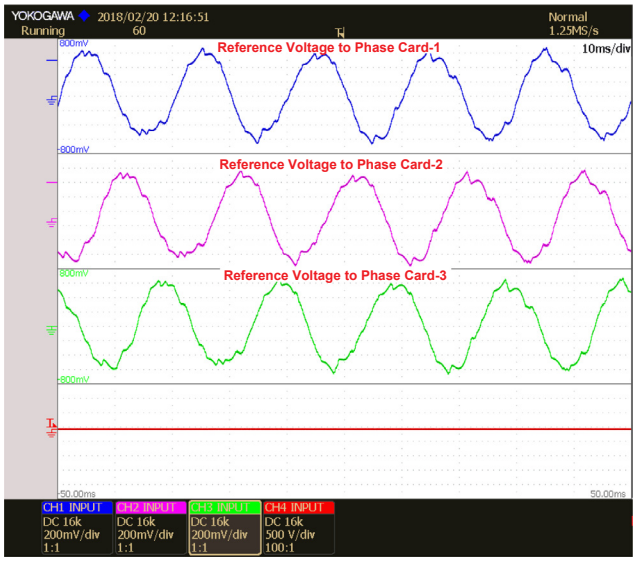

Fig. 23. Reference voltages generated Master Controller Card for Three Phase controller cards.

controller-in-loop simulations are carried out on a single phase five-level grid-connected PV power conditioning system in which Two numbers of Module-level controller cards are interfaced with one Phase-Level controller card as shown in Fig. 18. As explained earlier, the basic functionalities of the phase level controller card are determining the power reference for each H-Bridge module, obtaining reference voltage for each module and generation of a gate pulse for each H-Bridge module. In this setup, since the single-phase system is selected for controller in loop simulations, only one phase controller card is used and the functionalities of master controller are also incorporated in the phase controller card itself.

In controller in loop simulations, the simulated power circuit comprises of a cascaded 5-Level inverter which comprises of two cascaded H-Bridge modules fed from two isolated PV arrays is connected to a single phase 640 V Grid through an L-C-L filter and an AC contactor. The following activities are carried out during validation of phase controller card through controller-in-loop simulations.

- The power circuit is simulated, compiled and loaded in the CPU of the Real-Time simulator.
- Phase controller card is also loaded with the application programme.
- Each Module level controller is loaded with the control algorithm validated in the previous section.

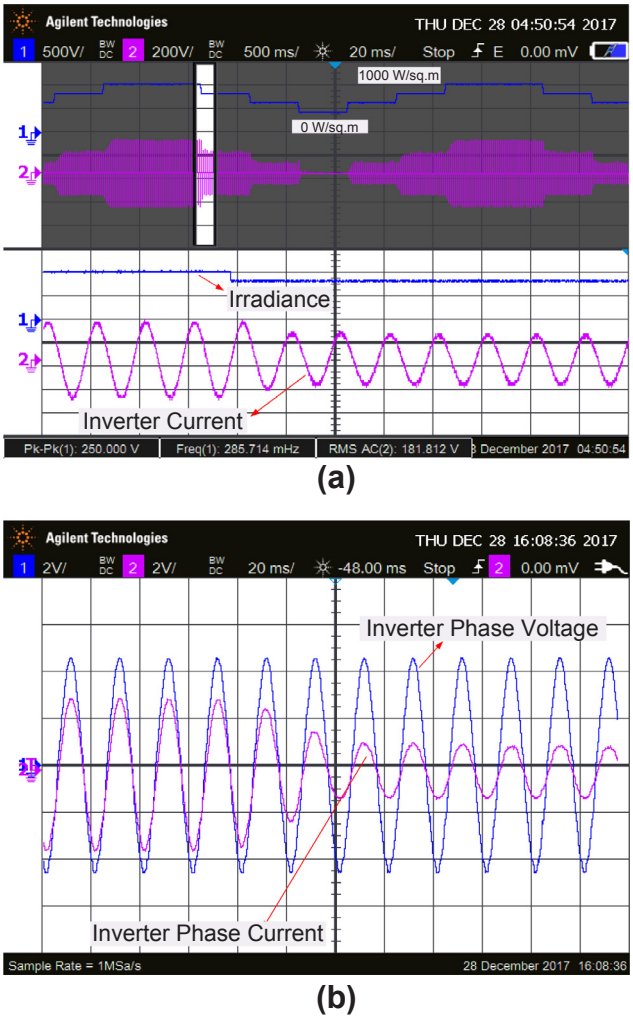

Fig. 24. Transient response of inverter current with change in Irradiance value.

- Connections are made between Phase level card and two module level controller cards for signal exchange.
- Irradiance values on two PV arrays are varied in steps. Two numbers of Analog output channels in the real-time simulator are assigned to monitor the irradiance values in an oscilloscope.
- Each Module level controller monitors the PV voltage and current for MPPT and generates 'Pinc' and 'Pdec' signals. The generated digital output signals are given to the phase controller.
- On receiving 'Pinc' and 'Pdec' signals from each module level controller card, the phase controller card generates the reference power value. The reference power value is given to two numbers of digital to analog converter (DAC) through a serial peripheral interface (SPI) of DSP. Outputs of DAC are given to the oscilloscope to monitor the reference power signals of each module.
- To monitor the values in an oscilloscope, Analog output channels in the real-time simulator are assigned for the signals such as output voltage of each H-Bridge module, RMS value of each H-Bridge module, PWM voltage of the inverter, Grid voltage, grid current, PV voltages, PV currents, etc..

Initially, system operation is validated by applying equal values of irradiance on both the PV modules and observed that the power references obtained for each module are equal as shown in Fig. 19(a). But in a practical case, since the arrangement of PV arrays spread over a huge area in a solar plant, irradiance on each PV array is not symmetrical. Sometimes, the difference in irradiance inputs on PV array may be huge due to partial shading and this may reduce the power output and may complicate the system operation [36]. With the proposed control architecture, the effects of partial shading can be minimized by carrying out independent MPPT controls of smaller PV arrays.

In this study, the system is tested by applying unequal values of irradiances on PV Array-1 and PV Array-2 and observed the reference powers for each H-bridge module are unequal and proportional to respective irradiance values as shown in Fig. 19(b). Power reference for the single phase CHB inverter is the sum of the reference powers obtained for each H-bridge modules. Current reference is obtained from the inverter reference power and the current controller gives the inverter reference voltage. The reference voltage for the H-bridge module is proportional to the reference power of the corresponding H-Bridge module. From the results shown in Fig. 19, it is evident that the performance of the system with the controls implemented in the phase level controller card is satisfactory during unequal irradiances and during partial shadings on PV arrays.

When irradiance values on each PV array are equal, then the reference power and in turn ac voltage output of each H-Bridge module are equal. Hence when the irradiances are equal the pulse width in PWM output voltages of H bridge-1 and H Bridge-2 are equal as shown in Fig. 20(a). When the irradiance values on both the PV arrays are not equal, then the module with higher irradiance will give PWM output with higher pulse width compared to the module with lower irradiance value. When the irradiance on the PV Array-1 is more than that of PV Array- 2, then the pulse width in PWM output voltage of H-Bridge module-1 is more than that of H-Bridge module-2 as shown in Fig. 20(b). Similarly, when the irradiance on the PV Array-1 is less than that of PV Array-2, then the pulse width in PWM output voltage of H-Bridge module-1 is less than that of H-Bridge module-2 as shown in Fig. 20(c). Since phase shifted PWM method is adopted, each H-Bride module provides a Two-Level output and due to the phase displacement between carrier signals, PWM output voltage of CHB inverter is of 5-Levels as shown in Fig. 20(d).

From the controller in loop simulation results presented, it is understood that independent voltage control of each H-Bridge module is possible with the software developed for the phase controller which enables independent power control of each PV-array. With the phase shifted PWM method adopted, all the H-bridge modules in the CHB inverter operate with almost equal duty cycle hence the switching losses for all the H-Bridge modules are identical. In this system, since only two H-Bridges per phase are considered; the phase faulty signal is not discussed. In this section, a single phase system is considered since the software for only one phase controller card is validated. The results obtained with the controls programmed in the phase level controller card are in line with the simulation results of independent MPPT controls of a CHB based inverter presented in Refs. [10,11] and the experimental results presented in Ref. [12]. Hence it is evident that the module level controller card, phase level controller card, and the associated control software are functioning properly when the number of H-Bridge modules are connected in cascade. In present work, PWM voltage waveforms for each H-Bridge module for different operating points are also studied and discussed.

5.3. Real-time simulation validation of master controller

To validate the functionalities of a master controller card, controller-in-loop simulations are carried out. In this setup, six numbers of module-level controller cards, three numbers of phase controller cards and one master controller card are used and are interconnected in line with earlier discussions. The master controller is connected to phase controller cards and also interfaced with the simulated power circuit through I/O channels of the real-time simulator as shown in Fig. 21. In controller in loop simulations, the simulated power circuit comprises of a three-phase cascaded H-Bridge inverter which comprises of two cascaded H-Bridge modules per phase fed from six isolated PV arrays. CHB

inverter is connected to three phase 1100 V Grid through an L-C-L filter and an AC contactor. A fixed resistive load is also connected to the Grid.

As explained earlier, the basic functionalities of the master controller card are providing the reference phase voltages to the respective phase controller cards and controlling the power control through the CHB inverter. The following activities are carried out during validation of master controller card through controller-in-loop simulations.

- The power circuit is simulated, compiled and loaded in the CPU of the Real-Time simulator.
- Each Module level controller and phase level controller card is loaded with the control algorithm validated in previous subsections.
- The master controller is loaded with the application programme.
- Irradiance values on all the PV arrays are maintained equal and are varied in steps.
- Each Module level controller monitors the PV voltage and current for MPPT and generates Pinc and Pdec signals. The generated digital output signals are given to the phase controller.
- On receiving Pinc and Pdec signals from each module level controller card, the phase controller card generates overall Pinc and Pdec signals and given to the master controller.
- Reference power/current is generated in the master controller from the Pinc and Pdec signals received from the three-phase controller cards.
- Through the current controller, three reference phase voltages are generated. These three reference voltages are given to the phase controller cards through Analog output channels in the master controller. These three signals are monitored in the oscilloscope.
- Analog output channels in the real-time simulator are assigned to monitor the values of inverter current, grid current for different irradiance inputs on PV arrays.

Irradiance inputs on all the PV arrays are varied in steps and the currents of the inverter, grid, and local load are monitored. Since a fixed local load is connected to the grid, the load current is always constant. When the irradiance is very low, the power available at PV array is almost zero; hence the total load requirement is fed by grid as shown in Fig. 22(a). When irradiance input is increased to 250 W/sq m, still the PV array power is not sufficient to feed the entire local load requirement. In this case, the grid and inverter provide the current required for the local load as shown in Fig. 22(b). When irradiance input is increased further to 750 W/sq m, the power available at the PV array is more than the local load requirement, hence the additional power is transferred to the grid, hence the grid current is negative (i.e. 180 degree out of phase) as shown in Fig. 22(c). The magnitude of inverter current, grid currents for different values of irradiance inputs at steady state are shown in Fig. 22(d) and observed that the inverter current is proportional to the irradiance inputs.

The three reference phase voltage signals generated by the master controller for a particular irradiance value are shown in Fig. 23 and transient response of inverter current for a sudden change in irradiance are shown in Fig. 24(a). From the presented results it is observed that the transient response of the system is satisfactory as there is a smooth transition in inverter current for a step change in irradiance. Since reactive power reference is adjusted to Zero, the power factor of the system is near to unity hence the inverter phase voltage and current are in phase with each other as shown in Fig. 24(b). From the presented results it is evident that the operation of the master controller card and the associated control software are in line with the requirement. It is also observed that the power controls programmed in the master controller card provided similar results from the simulated results of a quasi Z-source CHB MLI for PV applications presented in [37]. The results presented during the changeover of current from PV Inverter to Grid and vice versa at different irradiance inputs while feeding a fixed load are in line with the simulation results presented in Ref. [29]. The results obtained in the present work are compared with the findings of previous works and the improvements achieved are summarized in Table 5.

Table 5
Summary of improvements achieved through the proposed system.

SL.NO.	Parameter	Improvements with the present work
1	The response time of reference PV power for a step change in Irradiance input	From Fig. 19 of Ref. [34], it is observed that the settling time of PV power for a step change in irradiance input is around 300 ms with the improved Perturb and Observe method presented. The settling time achieved with the proposed controls in the present work is around 50 ms as shown in Fig. 16(a) and (b). Hence the MPPT controls implemented in the module-level controller provides better response time during transient conditions
2	Voltage spikes in Inverter PWM for sudden changes in inverter current	From the results shown in Figs. 10 and 12 of Ref. [13], voltage spikes in PWM output of CHB inverter is observed during sudden changes in the inverter output current To avoid such glitches in PWM voltage in the present system, MPPT controls are implemented to ensure a smooth transition in inverter reference power/current for sudden changes in irradiance inputs as shown in Fig. 16 of the present work. The proposed method helps in eliminating the voltage spikes in inverter PWM output as shown in Fig. 24(a)
3	Smooth Transition in current from Grid to Inverter and vice versa for sudden changes in irradiance	From Fig. 19(d), (e), (f) of Ref. [29], a smooth transition of current from Inverter to grid and vice versa is observed for a step change in current reference while feeding a constant load connected on the grid. In present work also; smooth transition in current is observed from Inverter to grid and vice versa for a step change in irradiance inputs on PV arrays as shown in Fig. 22
4	Phase Shifted PWM for CHB Inverter	Since Phase shifted PWM technique is used in present work for gate pulse generation, PWM outputs of each H-Bridge modules are identical as shown in Fig. 20(a) and are phase shifted by an angle depending on switching frequency and number of H-Bridge modules. Multilevel output voltage presented in Fig. 20(d) is obtained due to the phase difference between PWM voltages of H-bridge modules. The obtained results are in line with the simulation results shown in Figs. 4–7 of Ref. [11] and also are in line with the simulation results shown in Fig. 6(a) of Ref. [29]
5	Ripple content in inverter output current	From the experimental results shown in Fig. 19 of Ref. [29], it is observed that the ripple content in the output current of CHB based PV-Inverter is significantly more. With an improved filter design in the present work, the ripple content in the inverter output current is reduced as shown in Fig. 24
6	DC Link Voltage	From the simulation results shown in Fig. 4 of Ref. [11] and experimental results shown in Fig. 8 of Ref. [12], it is observed that DC link voltages of all H-Bridge modules are almost maintained constant at maximum power point voltage (Vmpp). Similarly in present work also, the DC link voltages of all H-bridges are almost equal and maintained at Vmpp as shown in Fig. 20. Hence the proposed MPPT controls help in maintaining DC link voltages constant during equal and unequal irradiance inputs on PV arrays
7	Power Factor	Since only active power is controlled through PV inverter, Output voltage and current are in phase with each other as shown in Fig. 9 of Ref. [10] and as shown in Fig. 7(a) of Ref. [37], hence the power factor is maintained at unity. By maintaining reactive power reference at Zero in this work; it is observed that the unity power factor operation is achieved as shown in Fig. 24 of the present work which is in line with the results presented in previous simulation studies
8	Validation through Controller-In-Loop Simulations	In Refs. [32,33] controller in loop simulations are carried out for Grid-Connected PV Applications. In these works, a single controller card is used to validate the control algorithm which is not suitable for high power applications as it helps in validating only control software. In present work, multiple controller cards in three stages are interfaced with the Real-Time simulator. The proposed method is complex but helps in validating both the control hardware and software in a real-time application

6. Conclusions

In this work, three-stage control architecture suitable for large-scale PV system based on a CHB inverter is presented. Controls at different stages are explained in detail. Real-Time simulations are carried out to validate the proposed controls. Since various functions of the system are distributed among three different cards; the hardware requirements of each processor card are minimized and the issues related to computational speed are eliminated. Dynamic response of the module level controls are found satisfactory as the settling time of the reference power signal is around 50 ms for change in irradiance input value of 250 W/sq mm. Since the MPPT controls are carried out independently at module level; overall processing time for MPPT controls in this system is much better than that of the systems with single processor card. From the presented results, it is evident that the independent voltage controls implemented in phase controller card ensure that the voltage output of each H-Bridge module to be proportional to the MPP power of the corresponding PV array. Hence independent MPPT controls for each PV arrays are achieved with the controls implemented in the phase level controller card. From the results obtained with the proposed controls, smooth transition of current from Grid to PV inverter and vice versa are observed during sudden changes in irradiance inputs on PV arrays. Controls implemented in Master controller ensure the balanced powers in three phase system. The results obtained from this work are compared with previous works and simulation studies and observed that the proposed control architecture provides an enhanced performance. The reactive power compensation feature incorporated in the master controller helps in operating the system as PV-STATCOM and this helps in improving the utilization factor of the system. As a future work, the proposed system can be extended for hybrid PV-Battery systems by incorporating controls for battery charging/discharging at module level controller card without modifying the controls on other controller cards.

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