

Low-Voltage-Ride-Through Control of a Modular Multilevel SDBC Inverter for Utility-Scale Photovoltaic Systems

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Abstract—This paper presents theoretical and experimental discussions on low-voltage-ride-through (LVRT) operation of a modular multilevel single-delta bridge-cell (SDBC) inverter intended for utility-scale photovoltaic (PV) systems. As the penetration of distributed generation from renewable energy sources connected to medium- and high-voltage grids increases, grid-tied inverters progressively need to abide to stricter grid codes, which demand measures to maintain reliability of the grid. The latest grid codes require inverters in generation systems to provide dynamic grid support in the event of grid faults by injection of a reactive current. This paper discusses two unique solutions for an SDBC inverter to enable dynamic grid support. One method is to inject a zero-sequence current through feedforward control within the inverter, and the other is by utilizing power from the distributed dc-dc converters. No negative-sequence current is injected into the grid in both cases. This paper also highlights the issue of voltage-sag transformation through delta-wye transformers and its effect on the LVRT capability of the SDBC inverter. Experimental results on a three-phase 12.6-kVA system prove that the SDBC inverter is capable of seamlessly operating through symmetric and asymmetric voltage sags.

Keywords—Low-voltage-ride-through, Delta-configured, Cascaded H-bridge inverter, Photovoltaics.

I. INTRODUCTION

The next-generation utility-scale photovoltaic (PV) systems aim at employing two-digit multi-MW inverters that are connected directly to medium voltage (MV) while featuring high efficiency, high reliability and easy scalability through modularity. Multilevel cascaded H-bridge inverters combined with solid-state transformer technology have in recent years drawn considerable interest in utility-scale applications [1]–[4]. The single-delta bridge-cell (SDBC) converter is a prominent circuit topology that has been applied to various grid-tied applications such as static synchronous compensators (STATCOM) and PV inverters [3]–[6].

Figs. 1 and 2 illustrate the differences between a contemporary utility-scale PV system based on low-voltage (LV) central inverters and a new one that is based on the modular multilevel SDBC inverter. The former requires a line-frequency LV/MV-transformer between the low voltage output of each central inverter and the medium-voltage collector running within the plant. Each central inverter has a low voltage, but high current output, and a switching frequency in the lower kHz-range,

therefore requiring a large output filter. When the modular multilevel SDBC inverter is connected directly to a medium-voltage bus, it requires only a single line-frequency transformer between the medium-voltage collector and the high-voltage (HV) grid. Even if the switching frequency of each bridge cell is lower than 1 kHz, the SDBC inverter can, due to its distributed and modular structure, achieve excellent power conversion with low harmonic content at the grid side, which requires no installation of additional harmonic or switching-ripple filters. It has been shown that the SDBC inverter using level-shifted pulsewidth modulation (LS-PWM) is particularly suitable for PV applications. The reason is that it can operate stably and with low harmonic distortion even when the power contribution from each bridge cell is severely imbalanced [4].

As the penetration of distributed generation from renewable energy sources in electricity networks advances, modern grid codes have been adapted to this development by demanding higher efforts from grid-connected inverters to maintain the reliability of the grid. German grid codes for connections to medium- and high-voltage grids have, as one of the earliest, adopted strict regulations for the inverters to provide static and dynamic voltage support, the so-called “ancillary grid support” [7]–[10]. During grid faults, grid-tied inverters are required to stay connected and support the grid voltage by injection of reactive current. This is referred to commonly as the low-voltage-ride-through (LVRT) requirement [11].

Various LVRT control methods for modular multilevel single-star bridge-cell (SSBC) inverters have been proposed in technical literature, albeit mostly for applications other than PV, such as STATCOMs, and battery energy storage systems [12]–[15]. Few publications have considered the reactive-current requirements imposed by modern grid codes. There are positive-, negative-, and possibly zero-sequence voltages in an imbalanced grid. As for SDBC inverters, it is important to ensure that additional power components generated by the negative-sequence voltage components do not cause any overvoltage in each bridge-cell capacitor or overcurrent in the SDBC converter during an LVRT event.

One of the most common LVRT control methods for SSBC inverters relies on feedback control to determine the zero-sequence-voltage reference that ensures balanced bridge-cell capacitor voltages in normal and grid fault conditions [12]. Other methods utilize proportional-plus-integral (PI) feedback control to balance the bridge-cell capacitor voltages by injecting both positive- and negative-sequence grid currents [13]. It has also been shown that negative-sequence injection can result

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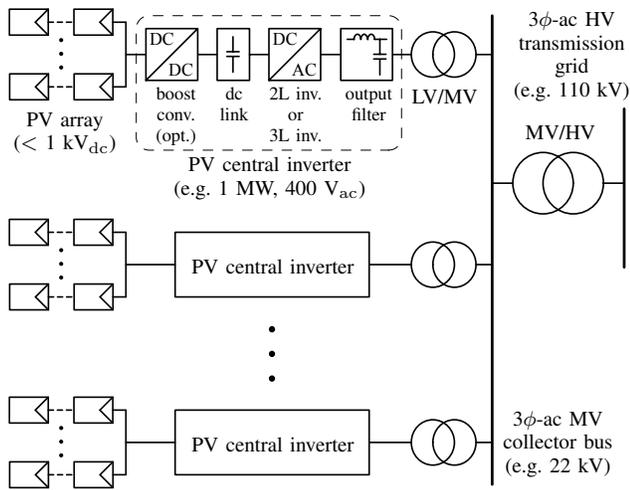


Fig. 1. Single-wire diagram of a contemporary utility-scale PV-system employing low-voltage PV central inverters.

in overcurrent or overmodulation, and the converter cannot maintain stability in certain situations [15]. The authors of [16] have analyzed the LVRT capability of an SDBC converter, utilizing both negative-sequence and zero-sequence current injection, but have not presented any general solution that does not require negative-sequence injection to maintain stability.

This paper presents theoretical and experimental discussions on a control strategy for ensuring the LVRT capability of an SDBC inverter in utility-scale PV systems. The dynamic behavior of the SDBC inverter is designed to comply with modern transmission-level grid codes that enforce dynamic grid-voltage support during grid-fault events. The proposed LVRT control employs a feedforward approach that relies on detecting positive- and negative-sequence grid-voltage components to calculate the required zero-sequence-current reference using a generalized formula. This paper presents two methods; one that relies only on the zero-sequence current, but may cause overcurrent for a short period of time, another that utilizes the available electric power from the dc-dc converters and allows mitigating the overcurrent issue.

II. DYNAMIC GRID-SUPPORT REQUIREMENTS

Fig 3(a) and (b) shows requirements for dynamic grid-voltage support during fault events for generating systems that connect to the high-voltage grid as described in the German *TransmissionCode* [8]. The corresponding technical guideline for medium-voltage networks [7] includes requirements that are similar to those for high-voltage networks. Initially, those requirements were valid only for symmetric three-phase faults, but have since been extended to include asymmetric one-phase and two-phase faults, after publication of the technical ordinance for wind-power generation systems [9].

Fig. 3(a) illustrates the simplified voltage-sag-over-time relationship that governs the ride-through requirements. The criterion to determine the depth of a voltage sag is the positive-sequence line-to-line voltage V_S^+ relative to the voltage in pre-sag conditions. Above the red line in Fig. 3(a), generating units such as inverters must stay connected for the time of the sag.

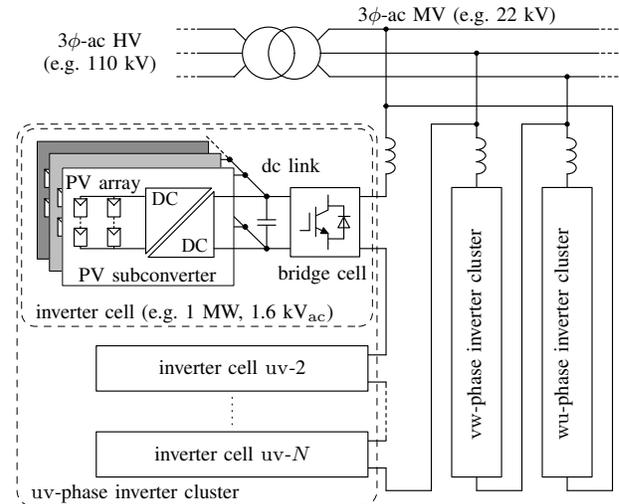


Fig. 2. Utility-scale PV system based on a modular multilevel SDBC inverter connected directly to a medium-voltage bus.

Fig. 3(b) presents the requirements for reactive-current injection during a grid fault. Grid codes require that the generation systems connected to medium- and high-voltage networks are capable of injecting capacitive positive-sequence reactive current for the case of voltage sags, and inductive positive-sequence reactive current for the case of voltage swells [7]–[9]. Injection of negative-sequence current components is usually suppressed during fault events. However, in recent years, in addition to positive-sequence reactive current, the injection of negative-sequence reactive-current components has been discussed with the aim of reducing negative-sequence components that appear in the grid voltage [17].

The latest technical guideline *VDE-AR-N 4120:2015* defines a set of requirements for injection of inductive negative-sequence reactive current during asymmetric one-phase and two-phase faults in addition to the already existing requirements for positive-sequence reactive-current injection [10]. This paper focuses only on positive-sequence reactive-current injection and suppresses negative-sequence current injection. Generally, grid codes allow the active current to be sufficiently reduced in favor of additional reactive-current injection with the aim of not exceeding the current capacity ratings of the generation systems [7]–[9]. After a fault is cleared, the generation systems should increase their active power at a defined maximum ramp rate.

III. SDBC INVERTER LVRT CONTROL

A. Circuit Configuration and DC-DC Converter Behavior

Fig. 2 shows that the SDBC inverter consists of three clusters in delta configuration, with each cluster employing N -cascaded bridge cells. One or more isolated dc-dc converters are connected to each bridge cell, which serve as an active interface between the PV array and the bridge cell. The dc-dc converters in this application have two modes of operation:

- maximum-power point-tracking (MPPT) mode
- constant-voltage mode

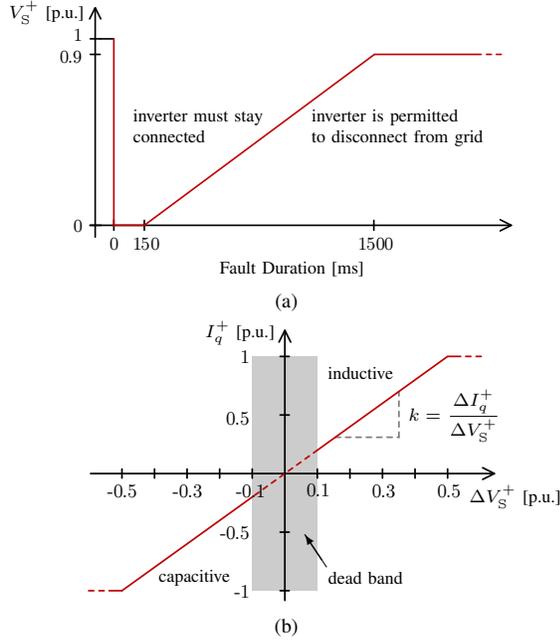


Fig. 3. Simplified LVRT requirements in German grid codes for generating systems connected to medium- and high-voltage grids [7]–[9]. (a) Voltage vs. fault duration curve. (b) Reactive current injection for dynamic voltage support.

In MPPT mode, the dc-dc converter extracts the maximum available power from the PV array and feeds it into the bridge-cell capacitor. MPPT is the normal mode of operation when no grid fault occurs. The dc-dc converter goes into the constant-voltage mode when the available power at the PV array side is higher than the average ac-power demand at the bridge-cell side. Therefore, the average bridge-cell capacitor voltage is kept constant. The dc-dc converter is assumed to be capable of only unidirectional power flow. This is the reason why the dc-dc converter has no means of sinking active power from the bridge-cell capacitor. During the event of a grid fault, when the SDBC output power is reduced, dc-dc converters switch to operate in the constant-voltage mode.

B. Generalized Zero-Sequence-Current Injection

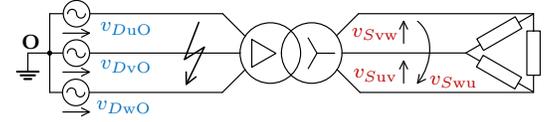
In order to obtain stable operation of an SDBC inverter during a voltage sag, bridge-cell capacitor voltages and cluster currents must be regulated within their limits. Moreover, the bridge-cell capacitor voltages must be balanced. Without loss of generality, this paper assumes the SDBC inverter is connected to the medium-voltage side of a delta-wye (vector group Dy11) transformer. Faults occur in the phase voltages at the high-voltage side and the phase voltages are:

$$\underline{V}_{DuO} = \frac{1}{\sqrt{3}} g_u V_D e^{-j\frac{\pi}{3}} \quad (1)$$

$$\underline{V}_{DvO} = \frac{1}{\sqrt{3}} g_v V_D e^{-j\pi} \quad (2)$$

$$\underline{V}_{DwO} = \frac{1}{\sqrt{3}} g_w V_D e^{j\frac{\pi}{3}}, \quad (3)$$

where g_u , g_v and g_w are coefficients describing the normalized voltage amplitudes and V_D is the nominal grid voltage



sag type	HV-grid side (delta)	MV-inverter side (wye)
1- ϕ sag (asymmetric) $g_u = 1$ $g_v = 1$ $g_w = 0.2$		
2- ϕ sag (asymmetric) $g_u = 1$ $g_v = 0.2$ $g_w = 0.2$		
3- ϕ sag (symmetric) $g_u = 0.3$ $g_v = 0.3$ $g_w = 0.3$		

Fig. 4. Visualization of voltage transformation through a delta-wye transformer in various cases of grid faults.

at the high-voltage side. The delta-wye transformer causes asymmetric voltage sags that occur on the high-voltage side to be transformed into voltage sags with different magnitude-phase relationships at the medium-voltage side.

Fig. 4 illustrates the transformation process using examples of one-phase, two-phase and three-phase voltage sags. The line-to-line voltages at the medium-voltage side are expressed, using the three scaling coefficients introduced in (1)–(3):

$$\underline{V}_{Suv} = \frac{V_S}{3} (g_u e^{-j\frac{\pi}{3}} + 2g_v + g_w e^{j\frac{\pi}{3}}) \quad (4)$$

$$\underline{V}_{Svw} = \frac{V_S}{3} (g_u + g_v e^{-j\frac{2\pi}{3}} + 2g_w e^{-j\frac{\pi}{3}}) \quad (5)$$

$$\underline{V}_{Swu} = \frac{V_S}{3} (-2g_u + g_v e^{-j\frac{2\pi}{3}} + g_w e^{j\frac{2\pi}{3}}), \quad (6)$$

where V_S is the nominal grid voltage at the medium-voltage side.

For further convenience, the set of unbalanced three-phase voltages is expressed in terms of their positive- and negative-sequence components:

$$\underline{V}_{Suv} = \underline{V}_{Suv}^+ + \underline{V}_{Suv}^- = V_S^+ + V_S^- e^{j\phi^-} \quad (7)$$

$$\underline{V}_{Svw} = \underline{V}_{Svw}^+ + \underline{V}_{Svw}^- = V_S^+ e^{-j\frac{2\pi}{3}} + V_S^- e^{j(\frac{2\pi}{3} + \phi^-)} \quad (8)$$

$$\underline{V}_{Swu} = \underline{V}_{Swu}^+ + \underline{V}_{Swu}^- = V_S^+ e^{j\frac{2\pi}{3}} + V_S^- e^{j(-\frac{2\pi}{3} + \phi^-)}. \quad (9)$$

Before, during and after a voltage sag, the three-phase SDBC inverter output currents are controlled to contain only positive-sequence components

$$\underline{I}_u = I^+ e^{j(-\frac{\pi}{6} + \theta)} \quad (10)$$

$$\underline{I}_v = I^+ e^{j(-\frac{5\pi}{6} + \theta)} \quad (11)$$

$$\underline{I}_w = I^+ e^{j(\frac{\pi}{2} + \theta)}. \quad (12)$$

TABLE I. ACTIVE AND REACTIVE CURRENT REQUIREMENTS

d_{sag}	I_d^+	I_q^+
$0 \leq d_{\text{sag}} < 0.1$	$\frac{P_{\text{avail}}}{\sqrt{3}V_S^+}$	0^*
$0.1 \leq d_{\text{sag}} < 0.5$	$\sqrt{(I_{\text{nom}})^2 - (I_q^+)^2}$	$-k d_{\text{sag}} I_{\text{nom}}$
$d_{\text{sag}} \geq 0.5$	0	$-I_{\text{nom}}$

* In this paper power factor (PF) = 1. In an actual system, PF $\in \{0.8 \dots 1\}$.

The SDBC inverter rms output-current $I^+ = \sqrt{I_d^{+2} + I_q^{+2}}$ is limited by the allowable output current rating. However, the inverter may permit some amount of overcurrent during the time of the voltage sag.

Table I summarizes the dq-axis current references as a function of d_{sag} . The depth of voltage sag is indicated as

$$d_{\text{sag}} = \Delta V_S^+ / V_S = 1 - V_S^+ / V_S, \quad (13)$$

which also determines the amount of positive-sequence reactive current that needs to be injected (see Fig.3 (b)). In normal conditions, the SDBC inverter operates in the MPPT mode by extracting the maximum available active power P_{avail} from the PV arrays. During a shallow voltage sag, a capacitive positive-sequence reactive current proportional to d_{sag} is injected. The active current is reduced, so that the nominal inverter output current I_{nom} is not exceeded. The proportionality factor $k \geq 2$ is normally provided by the transmission system operator [8]. In this paper, $k = 2$ is assumed.

The three-phase grid currents (10)-(12) are controlled as a result of controlling the three-phase cluster currents:

$$\underline{I}_{\text{uv}} = \underline{I}_{\text{uv}}^+ + \underline{I}_z = \frac{1}{\sqrt{3}} I^+ e^{j(\theta)} + I_z e^{j\phi_z} \quad (14)$$

$$\underline{I}_{\text{vw}} = \underline{I}_{\text{vw}}^+ + \underline{I}_z = \frac{1}{\sqrt{3}} I^+ e^{j(-\frac{2\pi}{3} + \theta)} + I_z e^{j\phi_z} \quad (15)$$

$$\underline{I}_{\text{wu}} = \underline{I}_{\text{wu}}^+ + \underline{I}_z = \frac{1}{\sqrt{3}} I^+ e^{j(\frac{2\pi}{3} + \theta)} + I_z e^{j\phi_z}. \quad (16)$$

The zero-sequence current \underline{I}_z is a degree of freedom that is used to transfer power among clusters without affecting the three-phase output currents [3]. During a voltage sag, unequal active power is generated among the three clusters as a result of the negative-sequence grid voltage V_S^- . To allow stable inverter operation, the power flow within each cluster should be balanced. Each cluster output power, generated by positive- and negative-sequence voltages and by positive- and zero-sequence cluster currents, must be equal to the corresponding input power P_{uv} , P_{vw} and P_{wu} from the dc-dc converters:

$$P_{\text{uv}} = \text{Re} \left\{ (V_{\text{Suv}}^+ + V_{\text{Suv}}^-) \overline{\underline{I}_{\text{uv}}} \right\} \quad (17)$$

$$P_{\text{vw}} = \text{Re} \left\{ (V_{\text{Svw}}^+ + V_{\text{Svw}}^-) \overline{\underline{I}_{\text{vw}}} \right\} \quad (18)$$

$$P_{\text{wu}} = \text{Re} \left\{ (V_{\text{Swu}}^+ + V_{\text{Swu}}^-) \overline{\underline{I}_{\text{wu}}} \right\}. \quad (19)$$

With the grid voltage, grid current, and dc input power given, the zero-sequence current is used to balance power among the three clusters. For this, both rms value I_z and phase angle ϕ_z , which are functions of eight variables need to be obtained:

$$\{I_z, \phi_z\} = f(P_{\text{uv}}, P_{\text{vw}}, P_{\text{wu}}, I^+, V_S^+, V_S^-, \phi^-, \theta) \quad (20)$$

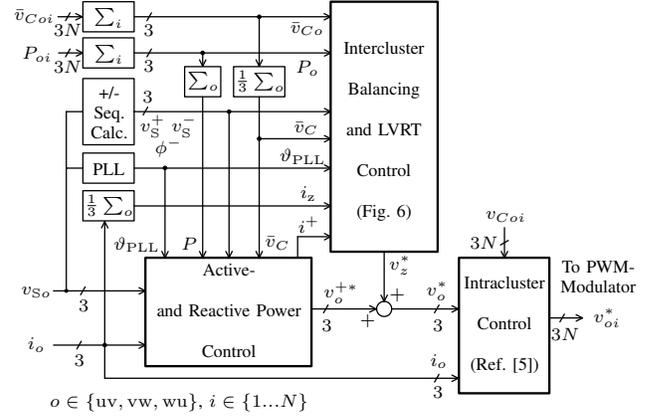


Fig. 5. Control block diagram of the SDBC inverter.

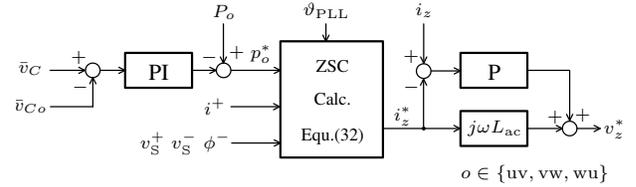


Fig. 6. Intercluster control and zero-sequence current control diagram.

Attempting to solve (17) to (19) leads to a system of two non-linear equations with two unknowns:

$$a_1 + a_2 I_z \cos(\phi_z) + a_3 I_z \sin(\phi_z) = 0 \quad (21)$$

$$b_1 + b_2 I_z \cos(\phi_z) + b_3 I_z \sin(\phi_z) = 0. \quad (22)$$

The six coefficients $a_x, b_x, x \in \{1, 2, 3\}$ are given by:

$$a_1 = P_{\text{uv}} - P_{\text{wu}} + \frac{I^+ V_S^-}{2} \times \left(\sin(\theta - \phi^-) - \sqrt{3} \cos(\theta - \phi^-) \right) \quad (23)$$

$$a_2 = \frac{1}{2} \left(-\sqrt{3} V_S^+ + V_S^- \sin(\phi^-) - \sqrt{3} V_S^- \cos(\phi^-) \right) \quad (24)$$

$$a_3 = \frac{1}{2} \left(V_S^+ - \sqrt{3} V_S^- \sin(\phi^-) - V_S^- \cos(\phi^-) \right) \quad (25)$$

$$b_1 = P_{\text{vw}} - P_{\text{wu}} + I^+ V_S^- \sin(\theta - \phi^-) \quad (26)$$

$$b_2 = V_S^- \sin(\phi^-) \quad (27)$$

$$b_3 = V_S^+ - V_S^- \cos(\phi^-). \quad (28)$$

By solving (21) and (22), a unique solution for I_z and ϕ_z can be obtained that allows direct calculation of the required zero-sequence current for any type of grid condition and any type of power imbalance situation:

$$I_z = -\frac{\sqrt{a_1^2 (b_2^2 + b_3^2) + b_1^2 (a_2^2 + a_3^2) - 2a_1 b_1 (a_2 b_2 + a_3 b_3)}}{\sqrt{3} |a_3 b_2 - a_2 b_3|} \quad (29)$$

$$\phi_z = \arg \left((a_3 b_1 - a_1 b_3) (a_3 b_2 - a_2 b_3) + j (a_2 b_1 - a_1 b_2) (a_2 b_3 - a_3 b_2) \right). \quad (30)$$

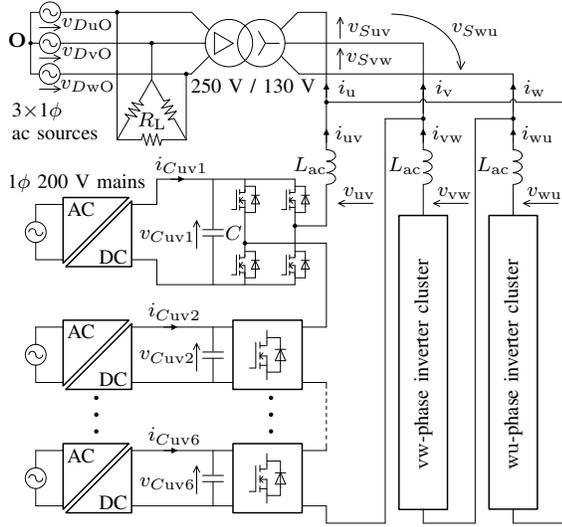


Fig. 7. Circuit configuration of the three-phase 130-V 12.6-kVA SDBC inverter with six bridge-cells per cluster and 18 individual dc-power converters.

C. Inverter Control

Fig. 5 shows the overall control strategy for the SDBC inverter to ride through voltage sags. It is characterized by a hierarchical structure consisting of three parts that are similar to SDBC inverters in different applications [6]. Fig. 5 includes a block that allows calculation of positive- and negative-sequence components from the three-phase grid voltages.

Fig. 6 depicts the control block diagram for the intercluster balancing control. It is responsible for handling the power exchange among the three clusters during normal and fault conditions by injecting a suitable zero-sequence current. The controller keeps the average bridge-cell capacitor voltages \bar{v}_{Co} , $o \in \{uv, vw, wu\}$ balanced by shifting excess power among the three clusters. The power reference p_o^* for each cluster includes the generated dc-power from the dc-dc converters P_o , and a term coming from the PI controller due to the deviation of each cluster's dc-capacitor voltage from the mean value:

$$p_o^* = P_o - K_2(\bar{v}_C - \bar{v}_{Co}) - \frac{K_2}{T_2} \int (\bar{v}_C - \bar{v}_{Co}) dt. \quad (31)$$

The zero-sequence current reference for an arbitrary operating condition is given by:

$$i_z^* = \sqrt{2}I_z \sin(\vartheta_{PLL} + \varphi_z), \quad (32)$$

with I_z and φ_z calculated from (29) and (30).

IV. EXPERIMENTAL SYSTEM AND CONTROL

Figs. 7 and 8 depict the circuit configuration used in the following experiments and the photograph of the experimental system. Table II summarizes its circuit parameters. A three-phase SDBC inverter with six bridge cells per cluster is combined with 18 isolated dc-power converters. Each of the 18 dc-power converters consists of a unidirectional galvanically isolated dc-to-dc converter and a front-end rectifier that is fed from a single-phase 200-V 50-Hz ac mains. Each dc-power



Fig. 8. Photograph of the three-phase SDBC inverter with six bridge-cells per cluster and 18 isolated dc-power converters used in experiments.

TABLE II. RATINGS AND SPECIFICATIONS OF THE SDBC INVERTER

Parameter	Symbol	Value
Nominal line-to-line voltage	V_S	130 V
Rated line frequency	$\omega_0/2\pi$	50 Hz
Rated apparent power	S	12.6 kVA
Cascade number	N	6
AC inductor	L_{ac}	0.43 mH (0.1 p.u.)
DC capacitor	C	46 mF
DC-capacitor voltage	V_{dc}	36 V
Unit capacitance constant	H	43 ms at 36 V
Load resistance	R_L	$3 \times 12 \Omega$
Modulation method		LS-PWM

Value in () is with respect to the rated power at nominal conditions.

converter allows a maximum output power of 1 kW, but the actual operating power per unit is set to 700 W, giving the SDBC inverter a rated capacity of 12.6 kVA.

Each dc-power converter allows two modes of operation: constant-voltage and constant-power mode. The constant-power mode emulates an MPPT operation of a dc-dc converter connected to a PV array in an actual system. In this constant-power mode, the output power from each dc-power converter $P_{oi} = v_{Coi} i_{Coi}$ ($o \in \{uv, vw, wu\}, i \in \{1..6\}$) is individually regulated to follow the given power reference P_{oi}^* , which is set to 700 W for each converter. If the average ac power output at the bridge-cell side becomes lower than the power reference due to a voltage sag, the dc-power converter switches operation to constant-voltage mode. The bridge-cell capacitor voltage is then kept at a constant value by providing active power on-demand. However, since the employed dc-power converters are unidirectional, they are incapable of actively sinking power from the bridge-cell capacitor.

The SDBC inverter is connected to the secondary side of a delta-wye transformer. The primary side is fed by three wye-configured single-phase ac-power-supply units and three delta-configured load resistors. Dynamically changing g_u , g_v and g_w allows the three ac power supplies to generate arbitrary voltage sags. The load resistors provide a means of sinking the active power produced by the SDBC inverter.

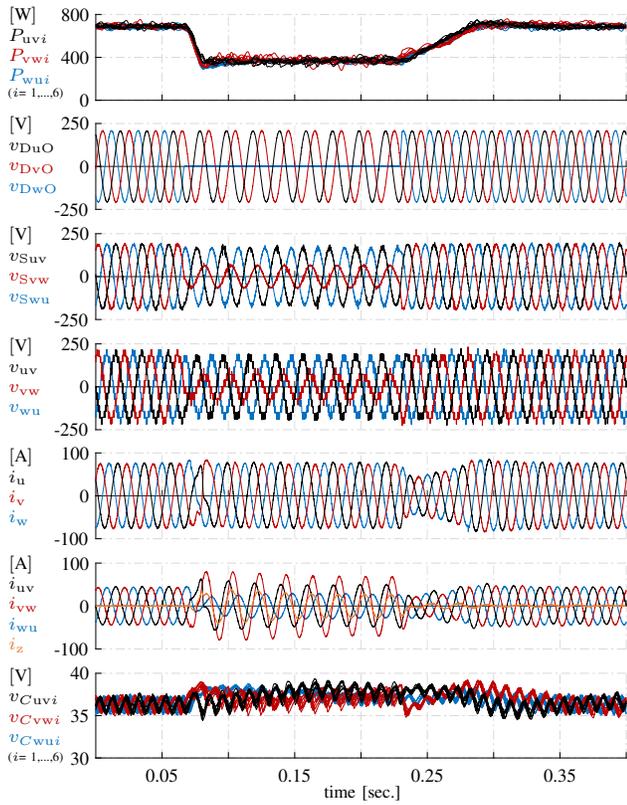


Fig. 9. Experimental waveforms of LVRT operation during a single-phase voltage sag to ground ($g_w = 0$). The active power from the dc-power converters reduces uniformly for all three clusters.

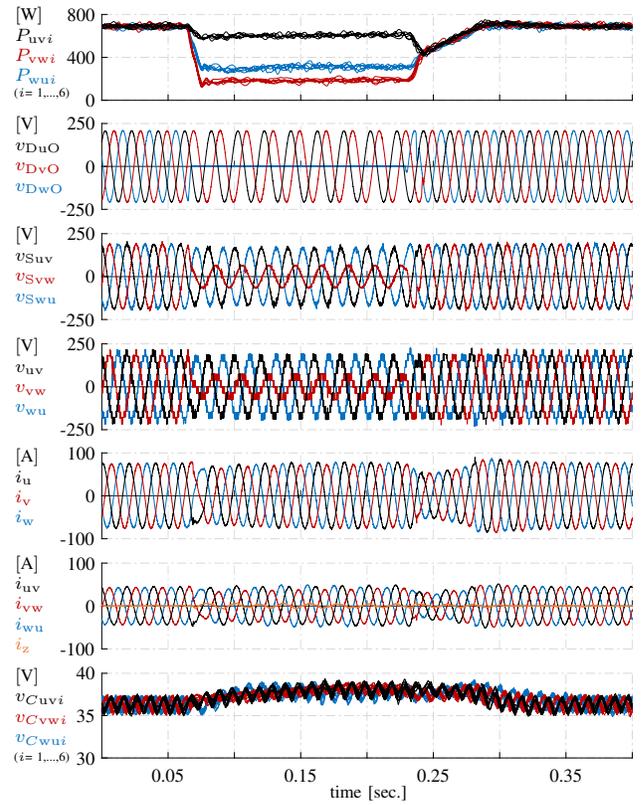


Fig. 10. Experimental waveforms of LVRT operation during a single-phase voltage sag to ground ($g_w = 0$). The active power from the dc-power converters reduces asymmetrically among all clusters making i_z almost zero.

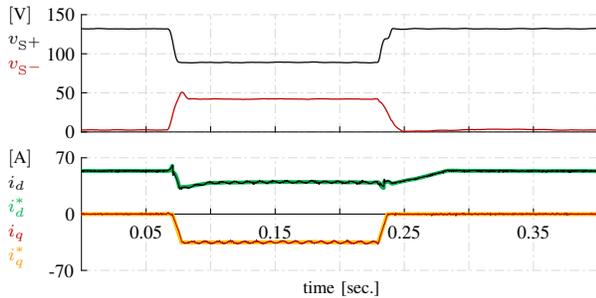


Fig. 11. Experimental positive- and negative-sequence voltages and dq-axis currents at the inverter output during a single-phase voltage sag (see Fig. 9).

V. EXPERIMENTAL RESULTS FOR VARIOUS GRID FAULTS

A. Single-Phase Voltage Sag To Ground

Fig. 9 shows experimental results of the SDBC inverter riding through a single-phase voltage sag. The voltage sag occurs in the w-phase ($g_w = 0$) at the primary side of the transformer, and results in a transformed asymmetric sag at the secondary side (see Fig. 4). Before the voltage sag, the inverter operates continuously at the rated conditions. During the voltage sag, capacitive reactive current is supplied to provide dynamic voltage support, while the active current is simultaneously reduced to limit the inverter output current to its nominal value. The reduction of the inverter output power results in an immediate increase in bridge-cell capacitor volt-

age. This causes the dc-power converters to switch operation from constant-power to constant-voltage mode.

In Fig. 9, it can be seen that the input power P_{oi} from the dc-power converters reduces equally among all three clusters¹. This is a direct result of the injected zero-sequence current that aims to balance the active-power generation among all three clusters. Despite the output current being within its rated limits, it is apparent that injection of the zero-sequence current leads to an increase in the cluster current by about 75% in cluster vw. Once the voltage sag is cleared, i_q is reduced to zero, and the output power is ramped up to its pre-sag value.

Fig. 10 presents experimental results under the same voltage-sag conditions as those in Fig. 9, but all of i_{uv} , i_{vw} and i_{wu} are kept within their nominal limits. This is possible because the SDBC inverter forces the dc-power converters to supply the required balancing power by limiting the zero-sequence current to almost zero. A reduction of I_z to zero is only possible if sufficient power is available at the PV generator side.

Fig. 11 illustrates the positive- and negative-sequence voltage components as well as the dq-axis currents and their references during the voltage sag in Fig. 9. It highlights the decoupled control of dq-axis currents during unbalanced grid-voltage conditions.

¹In Figs. 9-14, the 18 dc-power converter output powers P_{oi} are shown in averaged form after applying a low-pass filter with a cut-off frequency of 100-Hz. This filter serves only to improve visualization.

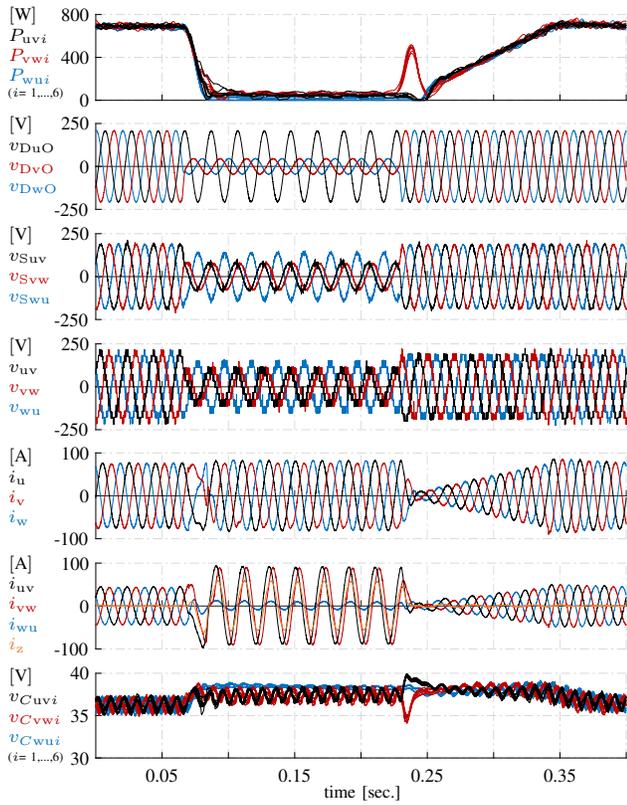


Fig. 12. Experimental waveforms of LVRT operation during a two-phase voltage sag to 2% ($g_v = g_w = 0.2$). The active power on the dc-power converter side reduces equally to zero for all three clusters.

B. Two-Phase Voltage Sag With 20% Voltage Remaining

Fig. 12 shows the SDBC inverter operating in a situation when v_{DvO} and v_{DwO} suddenly dropped to 20% of their nominal value. The depth of sag $d_{\text{sag}} \geq 0.5$ requires the SDBC inverter to inject capacitive reactive current at nominal capacity and reduce the active current to zero to limit the inverter output current to its nominal value. While the SDBC inverter output power is reduced to zero, the dc-power converters switch operation from constant-power to constant-voltage mode, effectively supplying only the required power to stabilize the bridge-cell capacitor voltages. This characteristic is apparent in Fig. 12 during the transient occurring at the time when the grid voltage suddenly recovered. The zero-sequence current causes a drop in the capacitor voltages of cluster vw, which quickly recovered after active power was supplied from the dc-power converters.

Fig. 12 makes it clear that i_{uv} and i_{vw} reach almost twice their nominal value as a result of the high amount of injected zero-sequence current. The large zero-sequence current is caused by the small phase-angle difference between v_{Suv} and v_{Svw} , which is a result of the voltage sag transformation (see Fig. 4). A small phase-angle difference leads to an increased demand of zero-sequence current to transfer excess power among clusters. It can be shown from (29) that a drop of g_v and g_w to zero causes v_{Suv} and v_{Svw} to coincide, which results in an infinitely large demand of zero-sequence current.

Fig. 13 shows experimental results under the same voltage-

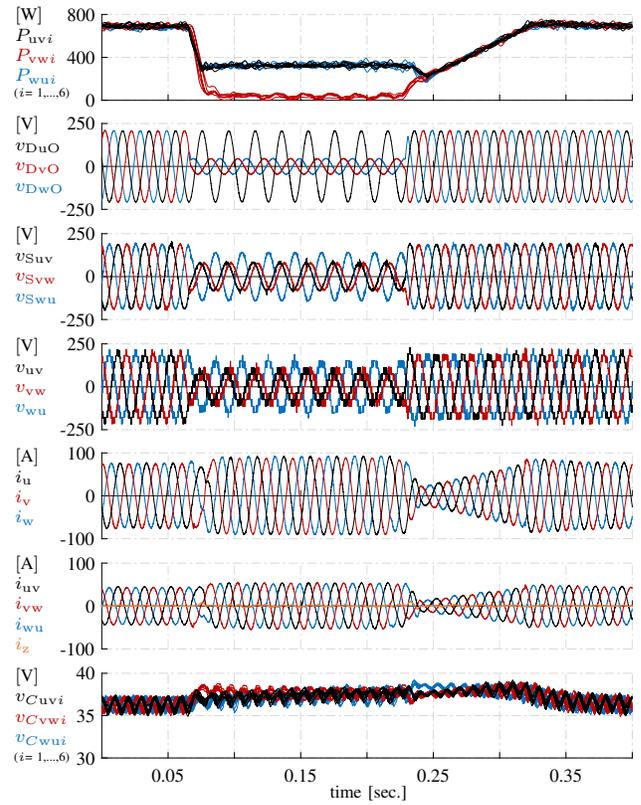


Fig. 13. Experimental waveforms of LVRT operation during a two-phase voltage sag to 2% ($g_v = g_w = 0.2$). The dc-power converters provide asymmetrically active power to make i_z almost zero.

sag conditions as those shown in Fig. 12, but without significant overcurrent. This operation is possible because satisfaction of (17) to (19) is established by supplying active power through the dc-power converters, instead of by transfer of power using the zero-sequence current. The zero-sequence current is almost zero and the unequal power demand of each cluster is satisfied by power from the dc-power converters. However, because the dc-power converters are unidirectional and cannot sink active power, any negative active cluster power that would otherwise be generated during the voltage sag, requires an offset of positive active power. This results in an inverter active-power output greater than zero and a grid current increase by about 15%, compared to that in Fig. 12.

C. Three-Phase Voltage Sag To Ground

Fig. 14 shows experimental waveforms of the SDBC inverter riding through a symmetric three-phase voltage sag to ground. During the time of the sag, I_d is reduced to zero and I_q^+ is increased to produce capacitive positive-sequence reactive current at nominal capacity. All dc-power converters are operating in constant-voltage mode and provide only enough active power to cover the inverter losses.

VI. CONCLUSION

This paper has provided theoretical and experimental discussions on the LVRT control of a modular multilevel SDBC inverter for utility-scale photovoltaic systems. The main focus

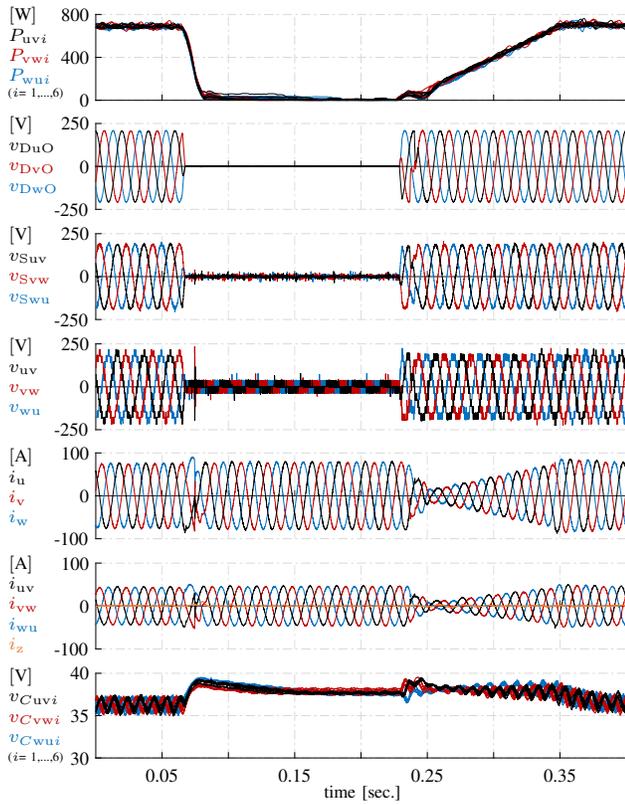


Fig. 14. Experimental waveforms showing LVRT operation during a symmetrical three-phase voltage sag to ground ($g_u = g_v = g_w = 0$).

of this research has been to establish stable operation with a continuous positive-sequence grid-current flow. This paper has shown that stable operation during symmetric and asymmetric voltage sags is possible without requiring injection of negative-sequence-current components for stability purposes. During fault conditions, the positive-sequence grid currents contain a capacitive positive-sequence reactive current as demanded by grid codes to provide dynamic grid-voltage support.

It has been shown that asymmetric voltage sags lead to an unequal active power distribution caused by negative-sequence grid voltages among the three clusters. A feedforward control method has been presented to allow calculation and injection of the required zero-sequence current for arbitrary grid-voltage and cluster-power imbalance situations. Experimental results from a downscaled three-phase 12.6-kVA SDBC inverter with six bridge cells per cluster have been presented to confirm the validity and effectiveness of the control.

This paper has found that although zero-sequence current injection has no negative impact on the three-phase balanced grid currents, it may, under certain conditions, increase the amount of rms cluster current beyond its rating. While an overcurrent of up to two times of its rated value for a time interval of less than one second may be well within the thermal limits of a practical system, this paper has presented and experimentally verified an alternative method that allows significant mitigation of cluster overcurrent during an asymmetric voltage sag. Instead of only relying on the zero-sequence current for the LVRT control, active power that is supplied by the dc-dc

converters can be utilized to stabilize the bridge-cell capacitor voltages and significantly reduce the amount of injected zero-sequence current that would otherwise be required.

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