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Comparative Analysis of Process Parameter Variations in DG-FinFET Device Using Statistical Methods

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Abstract. This paper investigates on the design and optimization of the input process parameter variations in Double Gate FinFET (DG-FinFET) device through comparisons between two different statistical methods through Taguchi and 2-k factorial design. This research focuses on the effects on threshold voltage (V_{TH}), leakage current (I_{OFF}), drive current (I_{ON}), and the subthreshold voltage (SS) towards various parameter variations. The fabrication of the device as well as its electrical characterization are both performed using TCAD simulator, specifically ATHENA and ATLAS modules. Optimization of the process parameters is implemented and merged with the aforementioned modules. The comparisons are also conducted for the Taguchi and 2-k factorial design, statistical methods after implementation is done for both. The optimum condition for the process parameters are obtained with Polysilicon Doping Dose at Level 3 (3.7E14 atom/cm^3), Polysilicon Doping Tilt at Level 3 (-17°), Source/Drain Doping Tilt at Level 1 (73°) and Threshold Voltage Doping dose at Level 2 (1.95E13 atom/cm^3). The S/N ratio of Threshold Voltage, Leakage Current, Drive Current and Subthreshold Voltage values are in the predicted range of the International Technology Roadmap for Semiconductors (ITRS) 2015 prediction. Based on comparisons made, optimization approach works best and most suitable with the Taguchi method due to the consideration of noise factor used in the orthogonal array, despite the fact that both Taguchi and 2-k factorial design process is able to produce optimum solutions that are within the desired values.

1. Introduction

The technological advancement in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology in microelectronic industry means that the reduction in its structure size is vital in producing a smaller, faster, cheaper yet optimized device for various applications to ensure a robust performance can be obtained. That being said, Moore's Law has been based on validating continuous scaling process of the MOSFET sizes [1]. Several issues such as short-channel effect (SCE) and drain induced barrier lowering (DIBL) have been faced as the scaling technology is advanced due to an incremental in process parameter variation in wafer fabrications [2,3]. The variations in process parameter have proven to play influential

yet significant role in determining optimum values of V_{TH}, I_{OFF}, I_{ON}, and SS. Therefore, optimizing the design cycle of the MOSFET can be managed through the implementation of statistical variations. Despite that, determining the connections between the electrical characterizations and process parameter variations are always proven to be a challenging [4]. The efficiency of the TCAD simulation design's robustness can be improved through the implementation of different statistical approaches [5-8]. The application of Taguchi method in process parameters optimizations has also been done by Salehuddin et al. and Afifah et. al. for 45 nm in obtaining desired V_{TH} and I_{OFF} values and 22 nm high-*k*/metal gate to obtain nominal V_{TH} and lower I_{OFF} values, respectively [9-14]. The impact of parameter variation on the circuit performance and its yield meanwhile, can also be reduced once information for the manufacturing process variations are adequately provided [15,16]. Thus, one of many statistical methods that are chosen to identify the process parameters besides the Taguchi method is through the realization of the 2-k factorial design.

2. Experimental Procedures

2.1. Device Fabrication using ATHENA

ITRS 2015 has predicted that the threshold voltage (V_{TH}) for the 19 nm gate length is within 0.461V to 0.510V [17]. The physical modelling of the nano-scaled device is acquired through simulation using Silvaco TCAD. Orientation of <100> is used in this design's main substrate which is a P-type silicon alongside an oxide layer grown on the top of the silicon bulk. By doing so, it acts as a mask during the P-well implantation process. This is followed by an injection of $1x10^{17}$ atom/cm^3 of Boron into the silicon substrate. Since the gate terminal can be separated from the source and drain terminal aside from its conductive channel through a dielectric layer, gate oxide is grown at 875ºC in the dry oxygen environment in 3% HCL at 1 atmospheric pressure. Meanwhile, the threshold voltage adjustment implantation is implemented in the channel region through approximately $1.95x10^{13}$ atom/cm^3 of Boron at an energy of 5 KeV. Significant changes can be observed once a slight adjustment being made towards the gate concentration and thus making it suitable to be considered as one of the parameter variations before the ones with most significant changes are opting. Polycrystalline silicon is then deposited on the semiconductor wafer as multi-layered structure is formed through the conformal polysilicon deposition. Meanwhile, as p-type impurities ion is implanted in the substrate that allows the formation of the n-type Source/Drain areas, indium is then doped with $1.17x10^{13}$ atom/cm^3 of dose with an implant energy of 1 keV in the halo implantation for which is able to reduce the SCE. The layer of nitride Si_3N_4 is produced on the surface of the silicon and polysilicon in sidewall spacer production. $1.22x10^{18}$ atom/cm^3 of arsenic dose with an implant energy of 3 keV is implanted in order to perform Source/Drain implantation before the side capacitance is minimized through compensate implantation. The first formation of the contact window in the Source/Drain region along with aluminium deposition and patterning has allowed the metallization process to be performed before structure mirroring process and electrode definition is made.

2.2. Significant process parameter identification and experiment setup

Finding shows that ten geometrical parameters that has been identified are not capable and enough to fulfil the optimization process as the structure of the device will differ through a slight alteration in the aforementioned parameters [18]. Therefore, six local variations parameters, which is from the process parameter fluctuations and two level of noise variations has been identified. Combination of parameters are severely needed for the statistical methods that are chosen to produce an optimized output response. Thus, all the significant parameters are chosen as in Table 1. Meanwhile, the noise factors that are used in this study are the Gate Oxidation Temperature and Polysilicon Oxidation Temperature that were assorted to get four output responses reading for each of the rows in the experiments which is output response 1 (Y1 Z1), output response 2 (Y1 Z2), output response 3 (Y2 Z1) and output response 4 (Y2 Z2).

Table 1. Process parameter levels

Symbol	Process Parameters	Unit
A	Polysilicon Doping Dose	Atom cm^{-3}
B	Polysilicon Doping Tilt	degree
C	Source/Drain Doping Dose	Atom cm^{-3}
D	Source/Drain Doping Tilt	degree
E	Threshold Voltage Doping Dose	Atom cm^{-3}
F	Threshold Voltage Doping Tilt	degree

The noise factor and its temperature levels are listed in Table 2. Consequently, the L_8 Orthogonal Array was used for Taguchi Method and L_8 Orthogonal Array for 2-k factorial method for which both methods are based on the total degree of freedom of the parameters.

Table 2. Noise factor levels

Symbol	Noise Factor	Unit	Level 1	Level 2
Y	Gate Oxidation Temperature	^oC	875 (Y1)	880 (Y2)
Z	Polysilicon Oxidation Temperature	^oC	875 (Z1)	880 (Z2)

2.3. Optimization of output response using L_8 (2^7) of Taguchi method

A total of eight experiments was operated for an L_8 (2^7) orthogonal array whereby four relevant process parameters and noise factors were acknowledged. Through eight experiments of the L_8 array, the complete response of the of V_{TH}, I_{OFF}, I_{ON}, and SS is obtained and Signal-to-Noise (S/N) ratio is used as it obtains the optimal parameters and also analyses the experimental data, where the larger S/N ratio, the better the characteristic performance is. In this statistical analysis, the S/N ratio for threshold voltage and drive current of the device attributes to the nominal-the-best and larger-the-better quality characteristics respectively. Apart from that, the S/N ratio for both leakage current and subthreshold swing of the device attribute to the smaller-the-best quality characteristic. The S/N ratio for nominal-the best quality characteristic is usually associated to a target output. In MOSFET's design, threshold voltage is always desired to be nominal in which most parts in MOSFET's operation heavily depend on the critical value of threshold voltage. Therefore, it is important to ensure that the threshold voltage of the designed device is tuned within an accepetable range, normally specified by chip manufacturers or predicted by the ITRS reports. The S/N ratio for larger-the-better quality characteristic is generally intended for having a larger ouput. In MOSFET's design, drive current is always desired to be as large as possible. A large drive current would significantly speed up the switching operation of the MOSFET due the faster gate voltage changes. The S/N ratio for lower-the-better quality characteristic is specifically aimed for having a smaller output. In this case, the leakage current and subthreshold voltage of the designed device are desired to be as small as possible. In regard with excessive leakage current, it is normally occurred to the MOSFETs that have ultra-small demensions in which the gate oxide is aggressively scaled down to reduce the parasitic capacitances. However, an extremely thin gate oxide would result in a larger leakage current due to less channel barriers for keeping the majority carriers from being leaked during off-state condition. In term of subthreshold swing, it is actually the behaviour of the drain current in the subthreshold region which its value is controlled by the gate terminal. The subthreshold swing is always desired to be as small as possible in order to achieve a perfect switch in which the MOSFET demonstrates a faster transition

between off (low current) and on (high current) states. S/N ratio chosen for the V_{TH} must be closer or equivalent to the nominal value of 0.455 V that is the mean from the ITRS 2015 specification set between 0.42 V to 0.49 V. The S/N ratio (SNR) which is for the nominal-the-best, ŋ can be expressed as (1). There are two factors in determining the nominal-the-best, which are dominant and adjustment factors [19]. Meanwhile, equations (4) and (5) expressing the respective smaller-the-best and larger-the-best characteristics. The ŋ (S/N) ratio for each of the experiments were calculated based on the equations (1), (4) and (5).

$$\text{ŋ} = 10\log_{10}[\mu^2/\sigma^2] \tag{1}$$

where

$$\mu = (Y_i + \cdots \ldots . + Y_n)/\text{n} \tag{2}$$

and

$$\sigma^2 = (\sum_{i=1}^{n}(Y_i - \mu)^2)/(\text{n} - 1) \tag{3}$$

$$n = 10\log_{10}[\tfrac{1}{n}\sum(Y_1^2 + Y_2^2 + \cdots + Y_n^2)] \tag{4}$$

$$n = 10\log_{10}[\tfrac{1}{n}\sum((1/Y_1^2) + (1/Y_2^2) + \cdots + (1/Y_n^2))] \tag{5}$$

The number of tests and the experimental values of the response characteristics each being represented by n and Y_n respectively. Through the equations applied, the S/N ratio obtained for each process parameter levels are summarized in Table 3. Similarly, the S/N response levels for the leakage current, drive current and subthreshold voltage is obtained through equations (4) and (5) for smaller-the-best and larger-the-best characteristics.

Table 3. Mean, variance and S/N Ratio for Double-Gate FinFET device

Experiment No.	V_{TH}				I_{OFF} SNR (Smaller-the-Best)	I_{ON} SNR (Larger-the-Best)	SS SNR (Smaller-the-Best)
	Mean	Variance	SNR Mean	SNR (Nominal-the-Best)			
1	0.433	5.40E-04	-7.26	25.41	-26.76	1.63	-38.98
2	0.506	7.82E-04	-5.91	25.15	-20.67	0.86	-39.08
3	0.479	3.94E-04	-6.40	27.65	-23.77	1.04	-39.11
4	0.534	7.28E-04	-5.45	25.92	-17.96	0.24	-39.16
5	0.505	7.60E-04	-5.93	25.26	-20.81	0.89	-39.08
6	0.431	5.48E-04	-7.31	25.30	-26.91	1.65	-38.99
7	0.534	7.42E-04	-5.46	25.84	-18.04	0.26	-39.16
8	0.477	3.95E-04	-6.42	27.61	-23.87	1.06	-39.08

2.4. Optimization of output response using L_8 (2^7) Orthogonal Array of 2-k fractional factorial method

The orthogonal array for the 2-k fractional factorial method as compared to the Taguchi method also comprises of a total of eight experiments operated for an L_8 (2^7) orthogonal array whereby four relevant

process parameters used in Taguchi method has been selected as in Table 4. The parameter's control factors may contribute to changes in device characteristics. Thus, the contrast analysis, effect estimation, variance effect estimation and sum of squares can be acquired through equations (6), (7), (8) and (9) respectively [20].

$$Contrast_{AB\ldots K} = (a \pm 1)(b \pm 1)\ldots(\mathrm{k} \pm 1) \quad (6)$$

$$AB\ldots K = 2/n2^{k}(Contrast_{AB\ldots K}) \quad (7)$$

$$Variance\ (Effect) = \left[1/2^{(k-1)}n^{2}\right]V(contrast) \quad (8)$$

$$SS_{AB\ldots K} = 1/n2^{k}(Contrast_{AB\ldots K})^{2} \quad (9)$$

Calculations of the analysis of variance for the 2-k factorial is completed by using Minitab software. The individual effects, coefficients and corresponding *t*-test has been acquired from the analysis of variance. Data analysis is then analyzed through effects estimation by using aPareto chart as in Figure 1 to Figure 4 whereby factor A, B, C, and D corresponds to the respective name given in A, B, C, and D.

Figure 1. Pareto Chart of the Standardized effect for threshold voltage

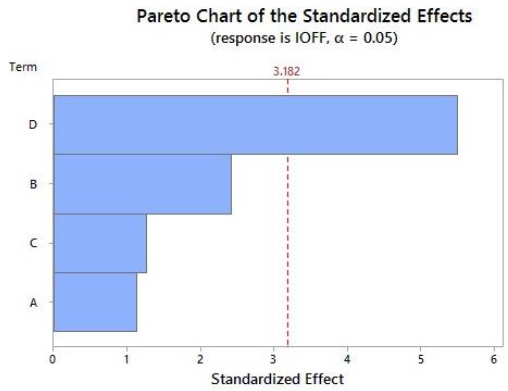

Figure 2. Pareto Chart of the Standardized effect for leakage current

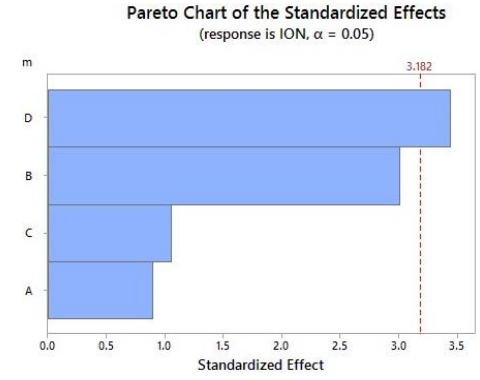

Figure 3. Pareto Chart of the Standardized effect for drive current

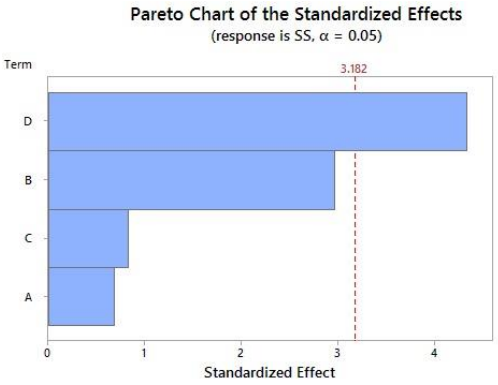

Figure 4. Pareto Chart of the Standardized effect for subthreshold voltage

Table 4. Input process parameter and their levels

Symbol	Noise Factor	Unit	Level 1	Level 2
A	Polysilicon Doping	atom cm^{-3}	3.60E+14	3.70E+14
B	Polysilicon Doping Tilt	degree	-15	-17
D	Source / Drain Doping Tilt	degree	73	74
E	Threshold Voltage Doping	atom cm^{-3}	1.95E+13	2.05E+13

3. Results and Procedures

3.1. Analysis of variance (ANOVA) for Taguchi method optimization

The variance decomposition which is the analysis of variance (ANOVA) allows the effect of different process parameter on the output response to be acquired. Meanwhile the percentages of factor effect on S/N ratio indicates the relative power of a factor to reduce variation, that being said the performance is greatly influenced by a factor with high contribution percentage. The chosen factor has been due to the high percentages of factor contribution as shown in Table 5. Table 6 shows the output response compared between the simulation and the estimation made by the ITRS 2015 whereby the results acquired in the simulation process proved to be highly correlated against the estimated results.

Table 5. Best combination of output response for Double-Gate FinFET Device.

Symbol	Process Parameter	Units	Best Optimization	
			Symbol	Value
A	Polysilicon Doping Dose	atom cm-3	A1	3.60E+14
B	Polysilicon Doping Tilt	degree	B2	-17
D	Source / Drain Doping Tilt	atom cm-3	D1	73
E	Threshold Voltage Doping Dose	degree	E1	1.95E+13

Table 6. Comparison of the best optimization between the estimated value, simulated value and the ITRS prediction.

	Optimum Condition			
	Estimation	Simulation	ITRS 2015 Prediction	Difference
Levels	A1 B2 D1 E1	A1 B2 D1 E1	-	-
V_{TH} (V)	-	0.479	0.455	0.0240
% Different from target Value	-	5.01	-	-
I_{OFF} (pA/μm)	-	7.77	< 20	2.00E-05
% Different from target Value	-	100.00	-	-
I_{ON} (mA/μm)	-	1.21	> 0.618	0.592E-03
Different from target Value	-	98.35	-	-
SS (mV/dec)	-	88.95	< 90mV/dec	1.05
Different from target Value	-	1.17	-	-

The optimum condition for all the output responses have been compared to choose the optimization value for the responses due to the percentages of the factor effect on S/N ratio that indicates the priority of a factor to reduce the variation. The confirmation test is done after the best output response combination is set so that the prediction accuracy is verified. The output responses at optimum combination of parameters and their levels was measured.

3.2. Analysis of variance (ANOVA) for 2-k fractional factorial method optimization

Generally, the effect of process parameter variations in ANOVA must be below than 0.05 in order to be considered as a significant factor based on the 95% confidence level. Conditionally, the factor with the significant value higher than 0.05 are ignored and the significance level below than 0.05 is listed in Table 7.

Table 7. Analysis of Variance

Item/Output Response	V_{TH} (V)	I_{OFF} (pA/μm)	I_{ON} (mA/μm)	SS(mV/dec)
DF	1	1	1	1
Adj SS	0.003762	172.345000	0.011073	4.788900
Adj MS	0.003762	172.345000	0.011073	4.788900
F-Value	18.93	30.20	11.85	18.82
P-Value	0.022	0.012	0.041	0.023

The optimum condition for all the output responses have been compared to choose the optimal value for the responses due to the percentages of the factor effect on significant value (p-value) that indicates the priority of a factor to reduce variation. The factor that has been chosen due to the high percentage contribution of each factor is listed in Table 8.

Table 8. Best combination of output response for Double Gate FinFET Device

Symbol	Process Parameter	Units	Best Optimization	
			Symbol	Value
A	Polysilicon Doping Dose	atom cm-3	A1	3.60E+14
B	Polysilicon Doping Tilt	degree	B2	-17
D	Source / Drain Doping Tilt	atom cm-3	D1	73
E	Threshold Voltage Doping Dose	degree	E1	1.95E+13

3.3. Comparisons between the results of different orthogonal array used for Taguchi Method and 2-k Factorial Method

In the DG-FinFET device, the Polysilicon Doping Dose at Level 1 (3.6E14 atom/cm^3), Polysilicon Doping Tilt at Level 3 (-17^o), Source/Drain Doping Tilt at Level 1 (73^o) and Threshold Voltage Doping dose at Level 1 (1.95E13 atom/cm^3) which is at A1 B2 D1 E1, respectively are the parameters optimum condition. The S/N ratio of Threshold Voltage, Leakage Current, Drive Current and Subthreshold Voltage value are in the predicted range of the ITRS 2015 prediction. The closer the value to the target, the better the quality of the process will be. Table 9 shows the comparison between the results of different orthogonal array used between Taguchi Method and 2-k Factorial Method. A small difference can be observed between the output responses. This indicates that the simulation value is using any of the orthogonal array is acceptable. From the results, it is concluded that, the number of experiments done does not affect the accuracy of the result. Both methods produce optimum solutions close to the desired value. Taguchi Method was observed to be more suitable to predict the real environment of the process due to the noise

factor that are used in the orthogonal array. The noise factor gives the additional robustness to the method that is most suitable to use and also requires less number of experiments based on the number of input process parameter (k) than the 2-k factorial method.

Table 9. The comparison between the results of different orthogonal array used for Taguchi Method and 2-k Factorial Method.

Outpur Response	Taguchi Method	2-k Factorial method	Difference	ITRS 2015 [17]
V_{TH} (V)	0.479	0.462	0.017	0.42 - 0.49
I_{OFF} (pA/μm)	15.21	18.75	3.54	< 20
I_{ON} (mA/μm)	1.129	1.176	0.047	> 0.618
SS (mV/dec)	90.23	88.51	1.72	< 90mV/dec

4. Conclusion

This research was to study the design and optimization of input process parameter variations in DG-FinFET device through comparisons between two different statistical methods through Taguchi and 2-k factorial design. An OA, SNR and ANOVA were utilized to study the performance characteristics of the Poly-Si/SiO_2 channel DG-FinFET device. Through the comparisons, it is observed that both statistical methods show the capabilities to optimize and improve the initial results for the device where all the device characteristics were observed to be closed to the prediction of ITRS 2015 requirement. Despite that, the Taguchi method was observed to have slight advantages over the 2-k factorial method in terms of the number of experiments required as the noise factor added to the Taguchi method has increased the robustness of the design whereby the V_{TH} is acquired within the range of the ITRS 2015 prediction for both Taguchi method (0.479 V) and 2-k factorial method (0.4618 V). Since the I_{OFF} is factored at "smaller-the-best", it is proven that the value is improved as low as 15.21 pA/µm compared to 2-k factorial method (18.75 pA/µm). However, the 2-k factorial method produces better results for I_{ON} which is at 1.1757 mA/µm compared to Taguchi (1.129 mA/µm) based on "larger-the-best" factor, as well as its SS which is relatively low for "smaller-the-best" optimization factor at 88.5069 mV/dec as compared to 90.23 mV/dec for Taguchi method. These results indicated that the L_8 OA of Taguchi method was capable of optimizing process parameter variations upon multiple device characteristics in DG-FinFET device. Thus, it was shown that the device characteristics with different performance characteristics can be simultaneously optimized where the V_{TH}, I_{ON} and I_{OFF} value for both devices meet the ITRS 2015 prediction for high performance logic multi-gate technology.

5. References

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