Modeling, Simulation and Optimization of 14nm High-K/Metal Gate NMOS with Taguchi Method

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***Abstract*— The developments in electronics technology push the invention of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) towards smaller physical dimension with improvements in both quality and performance. In this paper, design, fabrication and simulation of electrical characteristics of 14nm La_2O_3/WSi_2 NMOS is presented. The fabrication and simulation process of device were performed by using Virtual Wafer Fabrication (VWF) Silvaco TCAD Tools, which consists of ATHENA and ATLAS. The designed device was optimized using Taguchi Method that involves orthogonal arrays and analysis of variance (ANOVA). The original results before optimization process for V_{TH} is 0.212648V (7.5% lower than the targeted value) and I_{OFF} is $3.73851x10^{-9}$ A/µm while the optimized results for V_{TH} is 0.233321 V (1.44 % higher than the targeted value) and I_{OFF} is $4.732375x10^{-11}$ A/µm which fulfilled the targets based on International Technology Roadmap for Semiconductors (ITRS) 2013. The Taguchi optimization method yields a significantly lower I_{OFF} with an improved I_{ON}/I_{OFF} ratio by a factor of 25.**

Keywords—MOSFET, Taguchi, ATHENA, ATLAS

I. INTRODUCTION

In current fast paced technological era, the development of Si-based ultra large scale integrated circuits (ULSIs) have grown sharply for the last 40 years. The advancement of digitization and Internet of Things (IoT) will further increase the demand for semiconductors such as in smartphones, wearable electronics and IoT devices. The advancements in computer and software technologies have driven the invention of decreasing physical dimension, faster processing speed and reduce power consumption MOSFETs [1]. Thus, technological advancements on Si-ULSIs have provided tremendous computing power in ever device dimensions. Moreover, civilization is very much affected by nanotechnology and much of advancement of nanotechnology is embedded in conventional products of everyday life.

The increasing number of transistor count on ULSIs in the electronic devices has prompted the continued physical feature size scaling of MOSFETs by researchers. MOSFET in smaller physical dimension have higher efficiency, faster switching times, and lower production cost. The size of the MOSFET has to be scaled down to nanometer regime in order to compete in this challenging microelectronics industry while maintaining excellent functionality and quality.

Through scaling down the physical dimensions of MOSFET, the switching frequency increased with higher transistor drive current. Besides that, higher integration density could be achieved. However, negative effects such as Drain Induced Barrier Lowering (DIBL), and Hot Carrier Effect can affect performance and reliability [2]. All these effects will have impact on the leakage current (I_{OFF}) and will result in increased power consumption. Furthermore, the phenomenon of Short Channel Effect (SCE) occurs when the transistor device reaches nanometer regime. The charge distribution will be influenced due to the changes in electric field at the drain and source area. The SCE is attributed to the electron drift characteristics in the channel which results in modification of the threshold voltage (V_{TH}) [3].

High-k dielectric materials are being introduced as one of the control methods for gate oxide to resolve the problem of excess I_{OFF}. Furthermore, higher gate capacitance can be obtained at greater thickness by using high-k dielectric. Considerations on dielectric constant, large band gap and high band offset to silicon, stability, interface quality, process compatibility and reliability should be taken care of, when deciding for an alternative high-k dielectric material. Moreover, the selection of metal gate material with the considerations of matching work function and process integration paired with high-k dielectric material is critical for better performance [4].

In this paper, WSi_2 has been chosen as the metal gate material and paired with La_2O_3 dielectric in a NMOS due to its high thermal stability, high conductivity and high work function [4]. La_2O_3 gate dielectric has relative high permittivity and large band gap. Thus, it is able to reduce I_{OFF} and also enable the further scaling of gate oxide [5]. However, the use of high-k dielectric is quite challenging and difficult due to several issues such as interface control, unsuitable charge trapping causes V_{TH} instability, limiting scaling potential below 2 nm, thermal instability, significant mobility degradation and an unclear integration path [6].

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Taguchi experimental design is used in this research as statistical optimization method with the aim of identifying controllable factors which give significant impacts on the performance of NMOS. Orthogonal arrays (OAs) design is the statistical method proposed by Dr. Genichi Taguchi [7] to study the parameters with the least number of experiments. The fabrication process of NMOS transistor with the selected high-k material and metal gate was carried out virtually using ATHENA module while the device's electrical characteristics were characterized through ATLAS module [4]. Both modules are obtainable from the SILVACO TCAD simulator. The V_{TH} and I_{OFF} are the target values of the critical design characteristics that must be achieved.

II. PROCESS AND DEVICE STRUCTURE

A. Fabrication Process

The device was fabricated using ATHENA module. All the fabrication processes were based on similar research on the technology of High-K/Metal Gate [2]. However, design parameters were different since the doping concentrations were optimized according to the specifications of high-k dielectric material and metal gate that were used [8]. The design parameters of 14 nm NMOS is shown in Table I.

TABLE I. FABRICATION RECIPE OF NMOS

Process Step	Parameters
Silicon substrate	<100> orientation
Retrograde well implantation	200Å oxide layer by 970 ºC, 20 min of dry oxygen.
	$3.75x10^{12}$ atom/cm^2
	30 min, 900ºC diffused in nitrogen
STI isolation	130Å stress buffer by 900ºC, 25 min of dry oxygen
Gate oxide	diffused dry oxygen for 0.1 min, 815ºC
V_{TH} adjust implant	$2.7x10^{12}$ atom/cm^2 Boron difluoride
	5keV implant energy, 7º tilt
	20 min annealing at 800 ºC
High-K/Metal gate deposition	0.001um La_2O_3
	0.038um WSi_2
	30 min, 800ºC annealing
Halo implantation	$6.75x10^{13}$ atom/cm^2 Indium, 30º tilt
Sidewall spacer deposition	0.047um SiN
S/D implantation	$0.98x10^{14}$ atom/cm^2 Arsenic
	12KeV energy dopant, 7º tilt
PMD deposition	20 min, 852ºC annealing
Compensation implantation	$0.60x10^{14}$ atom/cm^2 phosphor
	60KeV energy dopant, 7º tilt
Metal 1	0.04 um Aluminum
IMD deposition	0.05 um BPSG
	15 min, 950ºC annealing
Metal 2	0.12 um Aluminum

After going through various processing steps in device fabrication, the cross section of the NMOS is depicted in Fig. 1. The NMOS has metal layer, oxide layer and semiconductor layer.

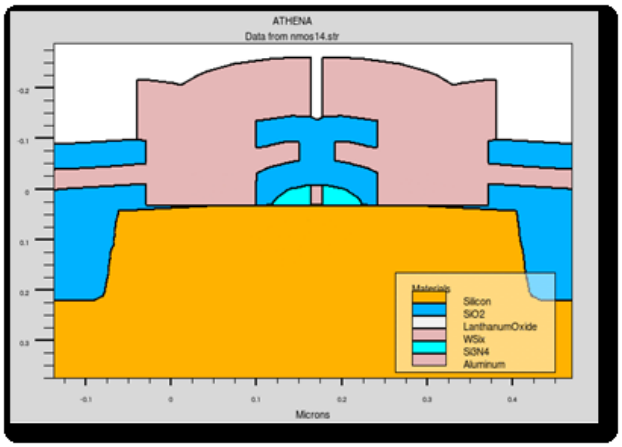

Fig. 1. Cross section of NMOS.

B. Taguchi L9 (3^4) Orthogonal Array Method

After the designed NMOS has been successfully fabricated and simulated, process parameters were optimized through Taguchi method by using experimental layout of L9 OA [9]. The values of the different levels of control factors are shown in Table II. Two noise factors (NF) were evaluated in the experiments as shown in Table III.

TABLE II. CONTROL FACTORS AND THEIR LEVELS

Control Factor	Unit	Level 1	Level 2	Level 3
Halo Implantation	atom/cm^2	$6.65x10^{13}$	$6.75x10^{13}$	$6.80x10^{13}$
Halo Tilt Angle	º	29	30	31
S/D Implantation	atom/cm^2	$0.97x10^{14}$	$0.98x10^{14}$	$1.00x10^{14}$
Compensation Implantation	atom/cm$_2$	$0.59x10^{14}$	$0.60x10^{14}$	$0.61x10^{14}$

TABLE III. NOISE FACTORS AND THEIR LEVELS

Noise Factor (NF)	Unit	Level 1	Level 2
Sacrificial Oxide Layer Temperature	ºC	910 (N1)	915 (N2)
Annealing Temperature	ºC	950 (M1)	949 (M2)

III. RESULTS AND DISCUSSION

A. Simulation of Electrical Characteristics

The designed NMOS was simulated in Silvaco TCAD in the ATLAS module. The simulation results for electrical characteristics of the NMOS are shown in Fig. 2 and Fig. 3.

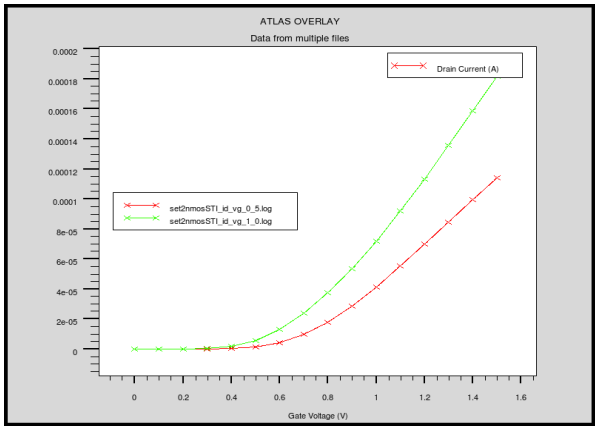

Fig. 2. $I_D - V_{GS}$ Curve

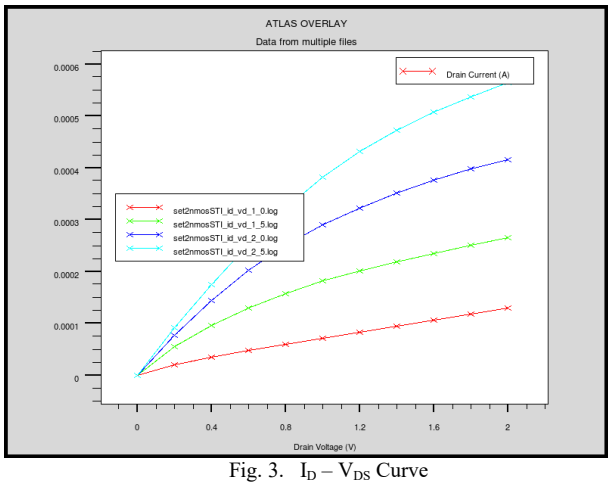

Fig. 3. $I_D - V_{DS}$ Curve

B. Optimization using Taguchi L9

Nine sets of different experiments for NMOS with 4 noise factors N1, N2, M1 and M2 were simulated according to the process parameter combinations as specified in the L9 OA. The simulation results for V_{TH} and I_{OFF} are shown in Table IV and Table V respectively.

TABLE IV. RESULTS OF VTH (V)

Exp. No	Threshold Voltage (V_{TH})			
	N1M1	*N1M2*	*N2M1*	*N2M1*
1	0.287137	0.323786	0.287239	0.323885
2	0.0824418	0.120627	0.0825364	0.12072
3	-0.1388	-0.10289	-0.138714	-0.10281
4	0.122842	0.158831	0.122936	0.158924
5	0.291788	0.329504	0.291888	0.329601
6	0.197709	0.237258	0.197802	0.237361
7	0.263194	0.303888	0.263295	0.303987
8	0.176829	0.212477	0.176922	0.212569
9	0.375447	0.412502	0.375544	0.412596

TABLE V. RESULTS OF IOFF (A/μM)

Exp No	Threshold Voltage (V_{TH})			
	N1M1	*N1M2*	*N2M1*	*N2M1*
1	1.29416×10^{-9}	7.83379×10^{-10}	1.29224×10^{-9}	7.82228×0^{-10}
2	2.88000×10^{-8}	1.63584×10^{-8}	2.87581×10^{-8}	1.63347×10^{-8}
3	8.07082×10^{-7}	4.89497×10^{-7}	8.06113×10^{-7}	4.88885×10^{-7}
4	1.54360×10^{-8}	9.04752×10^{-9}	1.54135×10^{-8}	9.03434×10^{-9}
5	1.22881×10^{-9}	7.3029×10^{-10}	1.22701×10^{-9}	7.29227×10^{-10}
6	4.63438×10^{-9}	2.64795×10^{-9}	4.62573×10^{-9}	2.64406×10^{-9}
7	1.87076×10^{-9}	1.07614×10^{-9}	1.86802×10^{-9}	1.07458×10^{-9}
8	6.48804×10^{-9}	3.80172×10^{-9}	6.47847×10^{-9}	3.79616×10^{-9}
9	3.41084×10^{-10}	2.00191×10^{-10}	3.40583×10^{-10}	1.99899×10^{-10}

Next was the process of finding the appropriate control factor levels to make the process less sensitive to variations in noise by studying the response variation using signal-to-noise (S/N) ratio. The optimal combinations were determined through signal-to-noise (S/N) ratio [4]. The level with the highest S/N ratio for each control factor was selected as to achieve better quality characteristic [10].

The quality characteristics in S/N ratio analysis are categorized into smaller-the-better (STB), larger-the-better (LTB) and nominal-the-best (NTB) performance characteristics [11]. V_{TH} analysis was determined by NTB characteristic while I_{OFF} analysis was determined by STB characteristic [12]. The S/N ratio for V_{TH} and I_{OFF} are shown in Table VI and Table VII respectively.

TABLE VI. S/N RATIO OF PROCESS PARAMETERS FOR VTH

Symbol	*Process Parameter*	S/N Ratio (Nominal-the-Best)			
		Level 1	*Level 2*	*Level 3*	*Total Mean S/N*
A	Halo Implantation	17.26	19.76	22.15	19.72
B	Halo Tilt Angle	20.48	18.63	20.06	
C	S/D Implantation	20.76	18.40	20.01	
D	Compensation Implantation	23.86	18.16	17.15	

TABLE VII. S/N RATIO OF PROCESS PARAMETERS IOFF

Symbol	*Process Parameter*	S/N Ratio (Smaller-the-Better)			
		Level 1	*Level 2*	*Level 3*	*Total Mean S/N*
A	Halo Implantation	151.86	168.78	177.63	166.09
B	Halo Tilt Angle	171.25	166.00	161.02	
C	S/D Implantation	171.13	167.22	159.92	
D	Compensation Implantation	183.47	165.80	148.99	

C. Analysis of Variance (ANOVA)

Analysis of variance (ANOVA) is a collection of statistical techniques used to analyze the percentage contribution of each individual control factor on the entire process [9]. Thus, ANOVA was used to determine the ranking of impact of the control factors towards V_{TH} and I_{OFF}. The ANOVA results for V_{TH} and I_{OFF} are tabulated Table VIII and Table IX respectively. The higher percentage on factor effect indicates the particular control factor contributes larger effect to the NMOS in terms of V_{TH} and I_{OFF}.

TABLE VIII. ANOVA ANALYSIS FOR VTH

Symbol	Process Parameter	Factor Effect	
		NTB	*Mean*
A	Halo Implantation	28	28.99
B	Halo Tilt Angle	4	2.40
C	S/D Implantation	7	3.53
D	Compensation Implantation	61	29.57

TABLE IX. ANOVA ANALYSIS FOR IOFF

Symbol	Process Parameter	Factor Effect
		STB
A	Halo Implantation	33
B	Halo Tilt Angle	5
C	S/D Implantation	6
D	Compensation Implantation	56

According to Table VIII, Compensation Implantation (D) has the most dominant factor effect while Halo Implantation (A) was identified as the adjustment factor, while Halo Tilt Angle (B) and S/D Implantation (C) acted as pooled factors for V_{TH}. For I_{OFF}, ANOVA was used to find the highest factor effect contribution by a control factor, namely the dominant factor for I_{OFF}. Thus, Compensation Implant (D) which has the highest factor effect was defined as the dominant factor as shown in Table IX.

D. Confirmation Test

Confirmation tests for both V_{TH} and I_{OFF} were carried out in the final phase of this work. The objective of the confirmation test is to verify the final results after optimization using Taguchi method [9]. The best setting for V_{TH} was defined as A1B2C2D1 while for I_{OFF}, it was A3B1C1D1. Table X shows the best setting of process parameters for confirmation runs performed for V_{TH} and I_{OFF}. Table XI and Table XII show the final results of confirmation test for V_{TH} and I_{OFF}.

TABLE X. BEST SETTING OF PROCESS PARAMETERS

Symbol	Process Parameter	Unit	Best Value	
			V_{TH}	I_{OFF}
A	Halo Implantation	atom/cm^2	6.65x10^{13}	6.80x10^{13}
B	Halo Tilt Angle	°	30	29
C	S/D Implantation	atom/cm^2	0.98x10^{14}	0.97x10^{14}
D	Compensation Implantation	atom/cm^2	0.59x10^{14}	0.59x10^{14}

TABLE XI. CONFIRMATION TEST RESULT OF VTH (V)

Noise Factor (N & M)				Best Value	
N1M1	*N1M2*	*N2M1*	*N2M2*	*NTB*	*Mean*
0.212935	0.253605	0.213038	0.253706	19.94	-12.64

According to ANOVA analysis and S/N ratio, the predicted S/N ratio for NTB falls between 14.27 dB to 22.01 dB. While the predicted S/N ratio for mean falls between -11.70 dB to -19.44 dB. This clearly shows that the obtained S/N ratio for NTB (19.94 dB) and mean (-12.64 dB) after optimization are in very good agreement with experimental. Furthermore, the average value of V_{TH} after optimization is 0.233321V (1.44 % higher than the targeted value).

TABLE XII. CONFIRMATION TEST RESULT OF IOFF (A/μM)

Noise Factor (N & M)				Best Value
N1M1	*N1M2*	*N2M1*	*N2M2*	*STB*
5.84952 ×10^{-11}	3.62233 ×10^{-11}	5.84065 ×10^{-11}	3.617 ×10^{-11}	206.5

According to Taguchi method, the predicted S/N ratio for STB falls between 179.78 dB to 220.34 dB. This shows that the obtained S/N ratio for I_{OFF} (206.5 dB) after optimization is within the predicted range. Besides, the average value of I_{OFF} after optimization is 4.732375x10^{-11} A/μm.

Through optimization process, the original result has been optimized from 0.212648 V (7.5% lower than the targeted value) to 0.233321 V (1.44 % higher than the targeted value) for V_{TH} and I_{OFF} from 3.73851x10^{-9} A/μm to 4.732375x10^{-11}A/μm. The average results after optimization for V_{TH} and I_{OFF} are shown in Table XIII and are compared with ITRS 2013 prediction.

TABLE XIII. AVERAGE RESULT OF CONFIRMATION TEST

Controlled Parameter	ITRS 2013 Prediction	Average Result
V_{TH} (V)	0.230±12.7%	0.233321 (+1.44%)
I_{OFF} (A/μm)	100 x10^{-9}	4.732375x10^{-11}

IV. CONCLUSION

This work has fulfilled the objectives and the simulation results have proven the possibility of fabricating 14nm La_2O_3/WSi_2 NMOS. Original results for the designed NMOS are 0.212648V for V_{TH} and 3.73851x10^{-9}A/μm for I_{OFF}. Then, Taguchi optimization was performed to optimize the process factors. The results obtained are compared with the predicted values of S/N ratio and ANOVA analysis. By using Taguchi method, the average V_{TH} of 0.233321V was observed with the control factors of A1B2C2D1. For I_{OFF}, the average value of 4.732375x10^{-11}A/μm was obtained. Therefore, this work has successfully demonstrated that La_2O_3/WSi_2 NMOS can be fabricated and optimized with both V_{TH} and I_{OFF} values fall within ITRS 2013 prediction.

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