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Configurations of memristor-based APUF for improved performance

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ABSTRACT

The memristor-based arbiter PUF (APUF) has great potential to be used for hardware security purposes. Its advantage is in its challenge-dependent delays, which cannot be modeled by machine learning algorithms. In this paper, further improvement is proposed, which are circuit configurations to the memristor-based APUF. Two configuration aspects were introduced namely varying the number of memristor per transistor, and the number of challenge and response bits. The purpose of the configurations is to introduce additional variation to the PUF, thereby improve PUF performance in terms of uniqueness, uniformity, and bit-aliasing; as well as resistance against support vector machine (SVM). Monte Carlo simulations were carried out on 180 nm and 130 nm, where both CMOS technologies have produced uniqueness, uniformity, and bit-aliasing values close to the ideal 50%; as well as SVM prediction accuracies no higher than 52.3%, therefore indicating excellent PUF performance.

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1. INTRODUCTION

1.1. Memory resistor

The memristor, short for "memory resistor", is the fourth fundamental passive circuit element; the first three being the resistor, capacitor, and inductor. The idea of the memristor falls on one of the six possible pairwise relationships among four fundamental circuit variables: current i, voltage v, charge q, and flux linkage Φ. Chua, in 1971, claimed that the q–Φ relationship is memristance, M [1-3] because, at the time, it was the only pairwise relationship left that was not yet firmly understood. These pairwise relationships are visualized in Figure 1 (left). Memristance, M, is simply resistance specifically for memristors, and is measured in ohms, Ω.

However, the actual memristor was only found in 2008 by HP Labs in their research for a suitable switch in their crossbar array [4, 5]. Their discovered memristor is made up of two layers of titanium dioxide, TiO2, where one layer is doped with oxygen vacancies, denoted as TiO2-x. The length of the doped layer is labelled w, whereas the length of the memristor is labelled D, where D is typically 10 nm. The structure of the memristor is shown in Figure 1 (right).

The memristor, as the name suggests, is a resistor with memory. Once the voltage across it is removed, the memristance at that time instance is retained. Also, the memristance increases over time until the maximum memristance, MOFF when connected at one polarity; and until the minimum memristance, MON at reverse polarity. The applied signal causes the oxygen vacancies in TiO2-x to move, whose direction depends on the polarity. Consequently, w changes and causes M to change as well. When the signal is removed, w is unchanged, and hence, M is retained [1-8]. The current-voltage i-v plot of the memristor

exhibits a pinched hysteresis loop when a sine signal is applied, as shown in Figure 2. The loop area shrinks with increasing frequency, and eventually reduces into a line as the frequency approaches infinity [1-8].

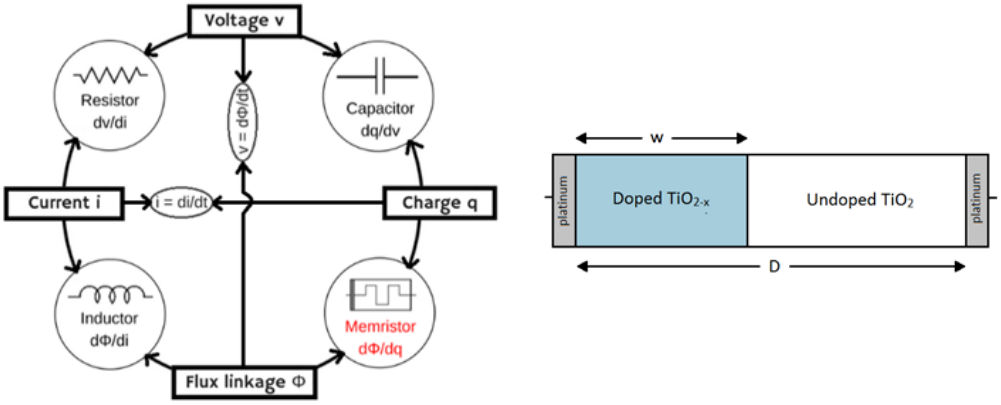

Figure 1. Pairwise relationship of the four circuit variables (left) and structure of HP memristor (right)

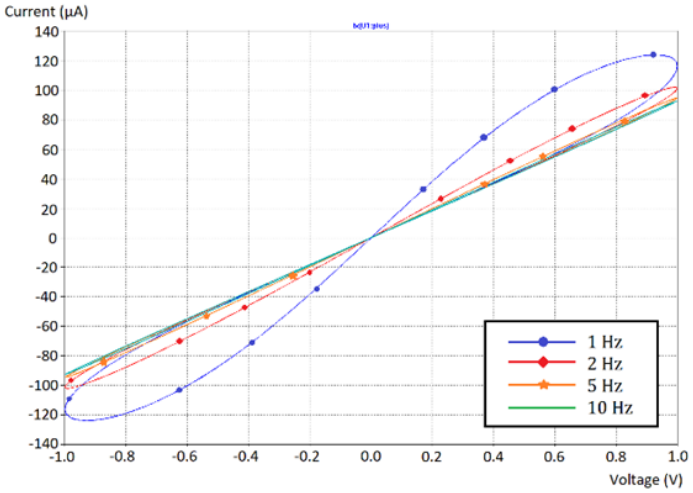

Figure 2. I-V plot of the memristor

The memristor is incorporated in PUF designs because of its memory-like properties and ability to change its memresistance which creates additional variation. Also, the memristor manufacturing technology is said to be relatively compatible with the modern CMOS fabrication standards [9]. In addition, the memristor-based PUFs have been conjectured to be more resistant to model building attacks than purely CMOS-based PUFs, because memristors are bidirectional devices as compared to the unidirectional MOSFET [10]. The memristor, roughly tens of nanometers long, is much smaller than most CMOS components and thus, reduces the area of the PUF. Hence, besides the APUF, other research efforts have been made to incorporate the memristor into different types of PUFs to enhance its performance [9-15].

1.2. Memristor based Arbiter PUF

The Physically Unclonable Function (PUF) was introduced for hardware security purposes [16-18]. The name PUF suggests that it is a physical circuit, which cannot be perfectly duplicated, that uniquely maps inputs to outputs. The input and output are termed as “challenge” and “response”, respectively. One mapping of a challenge to a response is termed as “challenge-response pair” (CRP). The PUF exploits manufacturing variations to have CRPs that are unpredictable (but repeatable), which are like unique “fingerprints”. This

unique "fingerprint" is inherent in the PUF circuitry and needs not be stored in memory. Hence, the PUF is used as an alternative to storing keys in nonvolatile memory in security applications like the identification and authentication of a device [19-21].

One PUF example is the memristor-based arbiter PUF (APUF), which was initially introduced by Mathew et al. [22] in Figure 3 (left). The advantage of this APUF over the traditional APUF is its challenge-dependent path delays which makes modelling by machine learning algorithms like SVM and LR infeasible [22]. The traditional APUF showed vulnerability such attacks up to 99% prediction accuracy [23-25].

Although the circuit design by Mathew et al. is resistant to attacks by machine learning algorithms, it was found to be susceptible to attacks by cryptanalysis, which was pointed out and circumvented by Chatterjee et al. by changing the transistor connection in the delay paths [26], as shown in Figure 3. Thus, the newer design has all its memristors affected in the challenge application stage, unlike the previous design where, depending on the challenge, only a subset of the memristors are affected.

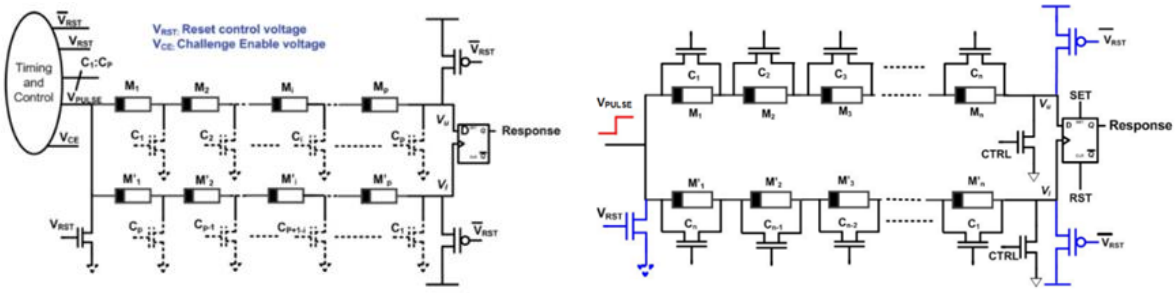

Figure 3. Memristor-based APUF by mathew et al. [22] (left) and by chatterjee et al. [26] (right)

Teo et al. made two modifications on the circuit design, which are adding arbiters to increase the number of response bits and replacing the D flip-flop with a SR NAND latch as the arbiter [27], as shown in Figure 4. The first modification is done because the SR NAND latch, compared to the D flip-flop has better input-to-output path symmetry, which reduces bias in the response generation. Also, the SR NAND latch is a simpler and smaller circuit component than the D flip-flop. As for the second modification, adding more response bits makes computing the response of the APUF more difficult, or at the very least, more time-consuming. Increasing the number of response bits from 1 to n results in the increase of the number of possible responses from 2 to 2n.

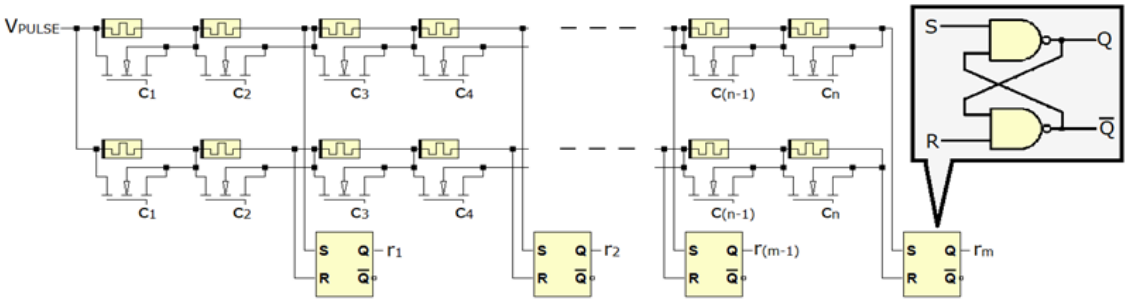

Figure 4. Memristor-based APUF by Teo et al. [27]

The operation of the memristor-based APUF can be briefly described in four stages [22, 26-27].

a. Reset: A reset signal, VRST, is set to 1. VRST is applied across all memristors to cause each memristor to be in its random initial memristance, which is dependent on the variations inherited in the manufacturing process.
b. Challenge application: VRST is set to 0. A pulse signal, VPULSE, and the challenge voltages are set to 1. Each memristor's memristance is altered in such a way that it is dependent on the applied challenge. Also, a control signal, VCTRL, is set to 1 to prevent the voltage at the input of the arbiters to rise and generate a false response bit.

c. Signal propagation: After a sufficient period, VCTRL is set to 0 to allow VPULSE to propagate to the arbiters.
d. Response generation: Depending on which of the two delay paths does the signal propagate faster, the output of the arbiter either maintains at 1 or toggles to 0, which is taken as the PUF response.

Based on the previous memristor-based APUF designs, further modifications can be made on the memristor-based APUF. Therefore, in this paper, circuit configurations are proposed as a means for increased variation and thereby, improve its performance in terms of uniqueness, uniformity, and bit-aliasing as well as resistance to SVM.

2. RESEARCH METHOD

2.1. Memristor-based APUF configurations

Configurations on the circuit of the memristor-based APUF are proposed simply to increase variation, thereby improve uniqueness and increase difficulty in duplication. The circuit designer may set the circuit of the memristor-based APUF to any desired, or even random, configuration so that it will be even more difficult for an adversary to duplicate the APUF without discovering the actual configuration. Take for example two APUFs that are both designed to be m-bit challenge and n-bit response. However, one of the APUFs may have more memristors per transistor, which has longer path delays than the other. Thus, both APUFs are more distinct from one another, besides already having variations due to the manufacturing process variations. In this paper, two configurations were made on the memristor-based APUF from two variables, which are number of memristors per transistor, and number of challenge and response bits.

The first configuration is varying the number of memristors per transistor. In other words, additional memristors are included in series between the source and drain terminals of each transistor. The memristor-based APUF was simulated from one to five memristors per transistor, where five memristors per transistor is shown in Figure 5. Each memristor added is subjected to manufacturing variations and thus, uniqueness can be improved.

As for the second configuration, the number of challenge bits is varied at 8, 16, and 32 bits, whereas the number of response bits is varied at 4 and 8 bits. Thus, there are a total of six possible combinations of challenge bits to response bits. The placement of the arbiters is spread out evenly along the delay paths. The position of the arbiters can be determined by simply dividing the number of challenge bits by the number of response bits. As an example, for 32 challenge bits and 4 response bits, the arbiters are placed on the delay paths after every eight transistors, as shown in Figure 6. For simulations in configuration 2, the number of memristor per transistor was fixed at one.

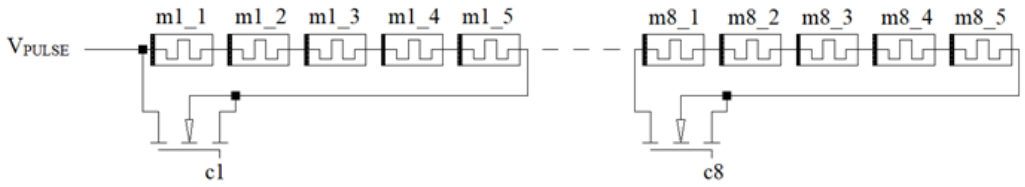

Figure 5. Example of configuration 1: 5 memristor per transistor

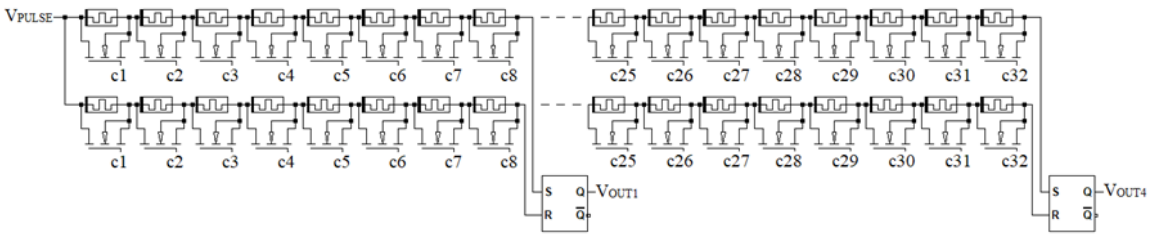

Figure 6. Example of configuration 2: 32-bit challenge, 4-bit response

2.2. Simulation setup

The circuit simulations were performed using SilTerra's 180nm at 1.8V and 130nm at 1.2V to observe any effect on the APUF performance. The memristor-based APUF circuit is based on Teo et al. [27]. The memristor SPICE circuit used is by Biolek et al. [28] with parameters shown in Table 1. The initial memresistance, MINIT, and the length of the memristor, D, were chosen as sources of manufacturing variation, set at 20% Monte Carlo variation of 5000 runs, similar to that performed in [22, 26, 27].

Table 1. Memristor simulation parameters

Memristor parameter		Value
Resistance at ON state	M_{ON}	100 kΩ
Resistance at OFF state	M_{OFF}	16 kΩ
Initial resistance	M_{INIT}	11kΩ (±20%)
Length of memristor	D	10nm (±20%)
Migration coefficient	μ	$10fm^2/(V{\cdot}s)$
Boundary control parameter	p	10

2.3. PUF Performance Metrics

The performance of the proposed memristor-based APUF is evaluated on uniqueness, uniformity, and bit-aliasing, which are metrics that have been derived by Maiti et al. [29]. The metrics were computed in MATLAB, where the following parameters are used.

a. x: number of PUF circuits tested
b. n: number of response bits
c. HD (Ri,Rj): Hamming distance of responses, Ri and Rj (where i and j are indexes)

Uniqueness estimates the ability of a PUF type to uniquely distinguish one circuit from another. Uniqueness is calculated by averaging all Hamming distances of all possible pairs of responses for the same applied challenge. The equation for uniqueness is shown in (1). The ideal value is 50% [29].

$$Uniqueness = \frac{1}{\binom{x}{2}} \sum_{i=1}^{x-1} \sum_{j=i+1}^{x} \frac{HD(R_i,R_j)}{n} \times 100\% \quad (1)$$

Uniformity measures the proportion of 0s and 1s of a PUF response, which indicates the presence of bias within the response. For the same applied challenge, let ri, j be the jth bit of the ith n-bit response (Ri), then the equation for calculating uniformity of the ith PUF circuit is given by (2). The ideal value is 50% to show a balanced proportion of 0s and 1s for one response [29].

$$Uniformity = \frac{1}{n} \sum_{j=1}^{n} r_{i,j} \times 100\% \quad (2)$$

Bit-aliasing measures the proportion of 0s and 1s for one bit-position of the responses. By letting ri, j be the jth bit of the ith n-bit response (Ri), the equation for calculating the bit-aliasing at the jth bit position is given by (2). The ideal value is 50% to show a balanced proportion of 0s and 1s for one bit position [29].

$$Bit-aliasing = \frac{1}{x} \sum_{i=1}^{x} r_{i,j} \times 100\% \quad (3)$$

2.4. Support Vector Machine (SVM)

Support vector machine (SVM), one of the widely used machine learning algorithms, is generally used to classify data. In the context of this research, SVM attempts to model the behavior of the memristor-based APUF. The SVM trains on a given subset of the CRPs, and then runs tests by predicting the rest of the CRPs. A good PUF should be able to resist being accurately predicted by any modeling attacks, and thus the desired outcome is 50% prediction accuracy, indicating that the SVM appears to be randomly guessing between 0 and 1, which is a sign that it cannot model the APUF. The training and testing of the CRPs were performed using the LIBSVM package [30]. The training set size was 50% of the CRP set, which were chosen at random and then, the rest of the CRP set is used for testing.

3. RESULTS AND ANALYSIS

3.1. Performance metrics

The simulation results of the memristor-based APUF for Configuration 1 on 180nm at 1.8V and 130nm at 1.2V are shown in Tables 2 and 3., respectively.

Table 2. Simulation results for configuration 1 on 180nm at 1.8V

No. of memristor per transistor	Performance metric (%)		
	Uniqueness	Uniformity	Bit-aliasing
1	49.998	49.940	49.938
2	50.008	49.795	49.900
3	49.995	50.310	50.344
4	46.886	50.335	50.388
5	50.011	49.905	50.088

Table 3. Simulation results for configuration 1 on 130nm at 1.2V

No. of memristor per transistor	Performance metric (%)		
	Uniqueness	Uniformity	Bit-aliasing
1	49.991	50.650	50.663
2	49.834	47.251	47.263
3	49.619	46.302	46.313
4	49.945	50.512	50.513
5	49.215	54.560	54.763

For both circuit simulators, the performance of the memristor-based APUF have shown improvement, that is the values of the performance metrics are much closer to 50% as compared to the results of other memristor-based APUFs in [26, 27]. Comparing between the results from both circuit simulators, 180 nm at 1.8 V presents a more favorable result. The discrepancy may be due to the difference in the CMOS technology used. Nevertheless, the results when the 130 nm at 1.2 V is used are still acceptable, which is within the ±5% range from the ideal 50%.

The simulation results for the configuration 2, which is varying the number of challenge and response bits are shown in Tables 4 and 5., for 180 nm at 1.8 V and 130 nm at 1.2V, respectively. The memristor-based APUF shows excellent performance regardless of the combination of the number of challenge bits or response bits used, especially for the simulation set using 180 nm at 1.8 V. However, there is a slight discrepancy for the case of 32 challenge bits and 4 response bits when using 130 nm at 1.2 V. Nevertheless, for the rest of the combinations, the results are still satisfactory.

Table 4. Simulation results for configuration 2 on 180nm at 1.8V

No. of challenge bits	Performance metric (%)					
	4 response bits			8 response bits		
	Uniqueness	Uniformity	Bit-aliasing	Uniqueness	Uniformity	Bit-aliasing
8	49.998	49.940	49.938	49.987	49.902	49.894
16	50.008	49.960	49.963	50.006	49.795	49.800
32	49.990	49.575	49.631	49.995	49.790	49.809

Table 5. Simulation results for configuration 2 on 120nm at 1.2V

No. of challenge bits	Performance metric (%)					
	4 response bits			8 response bits		
	Uniqueness	Uniformity	Bit-aliasing	Uniqueness	Uniformity	Bit-aliasing
8	49.991	50.650	50.663	49.719	47.376	47.375
16	49.338	44.903	44.875	49.695	47.889	47.881
32	42.460	66.692	66.700	48.775	56.833	56.838

The proposed configurations of the memristor-based APUF show favorable results in terms of the performance metric values, especially in the case of uniqueness for almost all configurations. These results show that the memristor-based APUF is more unique, or in simple terms, the PUF responses are not alike and predictable, and appear random. With that said, it is harder to observe a pattern or repeatability in the response bits to predict the response. Furthermore, the results are consistent regardless of the configuration used. Therefore, the memristor-based APUF maintains its resistance to possible attacks.

With configurations, the circuit designer has the freedom to set the memristor-based APUF into any desired, or even random, configuration, since there is no fixed rule on the configurations. It can be designed in such a way that both types of configurations discussed are applied. Therefore, it is more difficult for an adversary to duplicate a particular APUF without discovering the actual circuit design. In short, the memristor-based APUF, besides having improved performance in terms of uniqueness, uniformity, and bit-

aliasing, also has better reliability in the sense that the performance is unchanged with changing configurations.

3.2. SVM prediction accuracy

Tables 6 and 7 shows the accuracy of the SVM on configurations 1 and 2, respectively. The expected result is 50%, which is the probability of obtaining one out of two equally possible outcomes, like a fair coin toss. The results in Tables 6 and 7 shows very close to desired values for even a large training set. Therefore, the results indicate that the proposed configurations on the memristor-based APUF have strong resistance against attacks by SVM, which is one of the widely used machine learning algorithms.

Table 6. SVM prediction accuracy for configuration 1

No. of memristor per transistor	SVM prediction accuracy (%)
1	49.940
2	42.188
3	50.672
4	49.609
5	49.024

Table 7. SVM prediction accuracy for configuration 2

No. of challenge bits	SVM prediction accuracy (%)	
	4 response bits	8 response bits
8	51.913	52.344
16	50.586	48.731
32	49.024	48.731

4. CONCLUSION

In this paper, configurations on the memristor-based APUF are proposed to increase variations and thereby further improving the PUF performance in terms of uniqueness, uniformity, and bit-aliasing; as well as resistance to attacks by SVM. Also, it is to make it more difficult or time-consuming for an adversary to duplicate the circuit design. The configurations made are 1) varying the number of memristor per transistor, and 2) varying the number of challenge and response bits. The results show excellent performance as well as strong resistance against attacks by SVM. In addition, the results are consistent among configurations. The memristor-based APUF shows excellent simulation results for all configurations for both CMOS technologies. In conclusion, configurations can be used in the implementation of the memristor-based APUF as a device for hardware security.

Future research efforts will be focused on additional tests such as randomness using NIST test suite as well as using other machine learning algorithms like linear regression or artificial neural network. Eventually, the actual hardware implementation will be done.

ACKNOWLEDGEMENTS

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